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Performance of a New Monolithic Eight Channel Charge Sensitive Preamplifier-Shaper

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PERFORMANCE OF A NEW MONOLITHIC EIGHT CHANNEL CHARGE SENSITIVE PREAMPLIFIER-SHAPER

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A monolithic eight channel CMOS time-invariant preamplifier/shaper has been designed and built by Chuck Britton of ORNL in collaboration with Ray Yarema and Tom Zimmerman of Fermilab. Each of the eight channels incorporates a charge sensitive preamplifier and two shaping stages. The resultant weighting function is similar to $CR-RC^3$. The peaking time is approximately 200 ns, and the charge gain approximately in the range of 50-75 mv/fc. The layout was done on a Tinychip pad frame and the device was fabricated in a 2μ P-well process by Orbit. Figure 1 shows the chip layout. The channels are on an 84μ pitch in order to fit on a Tinychip without folding the layout. The design can be easily expanded to a larger number of channels.

This paper describes results of tests performed on this device at Fermilab. The tests were done with a bare die which was directly wirebonded to a printed circuit board. This minimizes parasitic effects which can become significant when using large packages. Results may be somewhat different when using the standard 40 pin package.

The top level schematic of the chip is shown in Figure 2. Figures 3, 4, and 5 are the preamplifier, first shaper, and second shaper, respectively, of each channel. The eight amplifiers share five common bias lines. Pin 12, Feedback Adjust, is the gate of a MOS transistor which is used as a high resistance to discharge the integrating capacitor. By applying a variable voltage source to pin 12, the resistance can be changed and the discharge rate varied. If the resistance is low enough, an undershoot is introduced into the output pulse. For testing, the voltage was adjusted so that no undershoot was introduced (about -0.6V). Pin 28, Peaking Time Adjust, is connected to another external variable voltage source and is used to vary the feedback resistance in the first shaping stage. This will affect the gain and peaking time of the amplifier. Pin 8, pin 7, and pin 31 are used to set bias currents for the amplifiers. The setup for these tests is as follows: pin 8 - $740K\Omega$ to Vss; pin 7 - $240 K\Omega$ to Vdd; pin 31 - $2.2M\Omega$ to Vdd. Pins 7 and 8 are also bypassed to ground with a 0.1 uf capacitor. Vdd and Vss are +4.5V and -4.5V, respectively.

The output of this chip has very limited drive capability, and is only intended to drive a high impedance, low capacitance load such as a FET probe. Thus for a practical system, some sort of output buffer is required very close to the channel output.

MEASUREMENT RESULTS

Peaking time, gain, equivalent noise charge, and DC offset were measured on all channels of two different chips, using a FET probe. The bias conditions were identical for all channels. Table 1 shows the results. In order to set the second chip's peaking time to be similar to that of Chip #1 (about 220 ns), the peaking time adjust must be changed from +2.25V to +2.50V. When this is done, the gain changes from 79 mv/fc to 67 mv/fc. In general, on a given chip, all channels are matched to within a few percent (peaking time and gain). From chip to chip, matching is not nearly as good. The Peaking Time Adjust can be used to compensate for this somewhat. However, this adjustment affects both peaking time and gain.

All further results are given for Chip #1 only.

Chip #1 results; $C_{in}=10\text{pf}$, $Q_{in}=5\text{fc}$, Peaking Time Adjust=+2.25V:

<u>Ch.#</u>	<u>Peak time</u>	<u>Gain (mv/fc)</u>	<u>ENC (e)</u>	<u>Vout DC (mv)</u>	<u>Vin DC (V)</u>
1	216 ns	73.6	960	+7	-1.225
2	220	74.5	970	+52	-1.219
3	220	74.8	940	+78	-1.251
4	212	72.6	940	-50	-1.262
5	208	74.1	900	+225	-1.289
6	not working				
7	216	75.3	930	+324	-1.274
8	212	72.8	990	+17	-1.239

Chip #2 results; $C_{in}=10\text{pf}$, $Q_{in}=5\text{fc}$, Peaking Time Adjust=+2.25V:

1	240 ns	79.3	900	+43	-1.290
2	244	79.0	920	+126	-1.260
3	248	79.8	910	+35	-1.289
4	244	78.6	900	+109	-1.280
5	244	77.6	880	+68	-1.301
6	236	76.4	900	-42	-1.292
7	240	78.4	910	+114	-1.278
8	244	81.0	930	+56	-1.265

Table 1.

Figure 6 shows the pulse response for different input capacitances. The response has been averaged to remove random noise. Note that for $C_{in}=5\text{pf}$, the Peaking Time Adjust has been changed to optimize the pulse shape and avoid ringing.

Noise measurements were made on one channel (Ch. 2) with varying input capacitance. The results are in Table 2. The slope is approximately 70 electrons/pf.

<u>C_{in} (pf)</u>	<u>Pk. time Adj. (V)</u>	<u>ENC (e)</u>
0	3.06	330
1	3.06	400
5	3.06	700
10	2.25	970
20	2.25	1620

Table 2.

For a given input capacitance of 10 pf, the Peaking Time Adjust was varied to check the range of feasible peaking times. Table 4 contains the results. The base to base width of the pulse stayed fairly constant (about 1 us). For voltages less than 1.9 V, ringing appeared in the pulse tail.

<u>Pk. time Adj. (V)</u>	<u>Pk. time (ns)</u>	<u>Gain (mv/fc)</u>
+4.5	144	30.1
+3.5	168	40.5
+2.5	204	63.1
+1.9	256	96.2

Table 4.

The dynamic range was measured for both signal polarities. Results are in Table 5. A 47K resistor was added from the output to -4.5V in order to help the pulldown capability. There is a 4% linearity error between +5 fc and +20 fc.

<u>Q_{in} (fc)</u>	<u>V_{peak} (mv)</u>
+5	+241
+10	+489
+20	+1003
+28.3	+1448
+40	saturates
-5	-233
-10	-457
-20	saturates

Table 5.

The adjacent channel crosstalk was measured to be about 1%. Power dissipation is 1.2 mw/ch.

CONCLUSION

An eight channel charge sensitive preamp/shaper has been designed which can be used for a variety of applications. The impulse response of the preamplifiers is dependent on the input capacitance, and has a peaking time in the range of about 150-250 ns. Noise increases with input capacitance at an acceptable 70 electrons/pf. Noise in a packaged part will be increased due to the estimated 2-3 pf of parasitic input lead capacitance.

Channel to channel peaking time and gain are uniform to within 5% on a given chip. Chip to chip variations are larger. Some compensation for this is possible by virtue of the Peaking Time Adjust, which varies the peaking time and the gain of all channels on a chip. However, these two quantities cannot be varied independently.

The present chip was designed as a test chip and has minimal output drive capability. A follower stage is needed in most practical applications. This follower could easily be added in future designs.

bvx3_8_chip

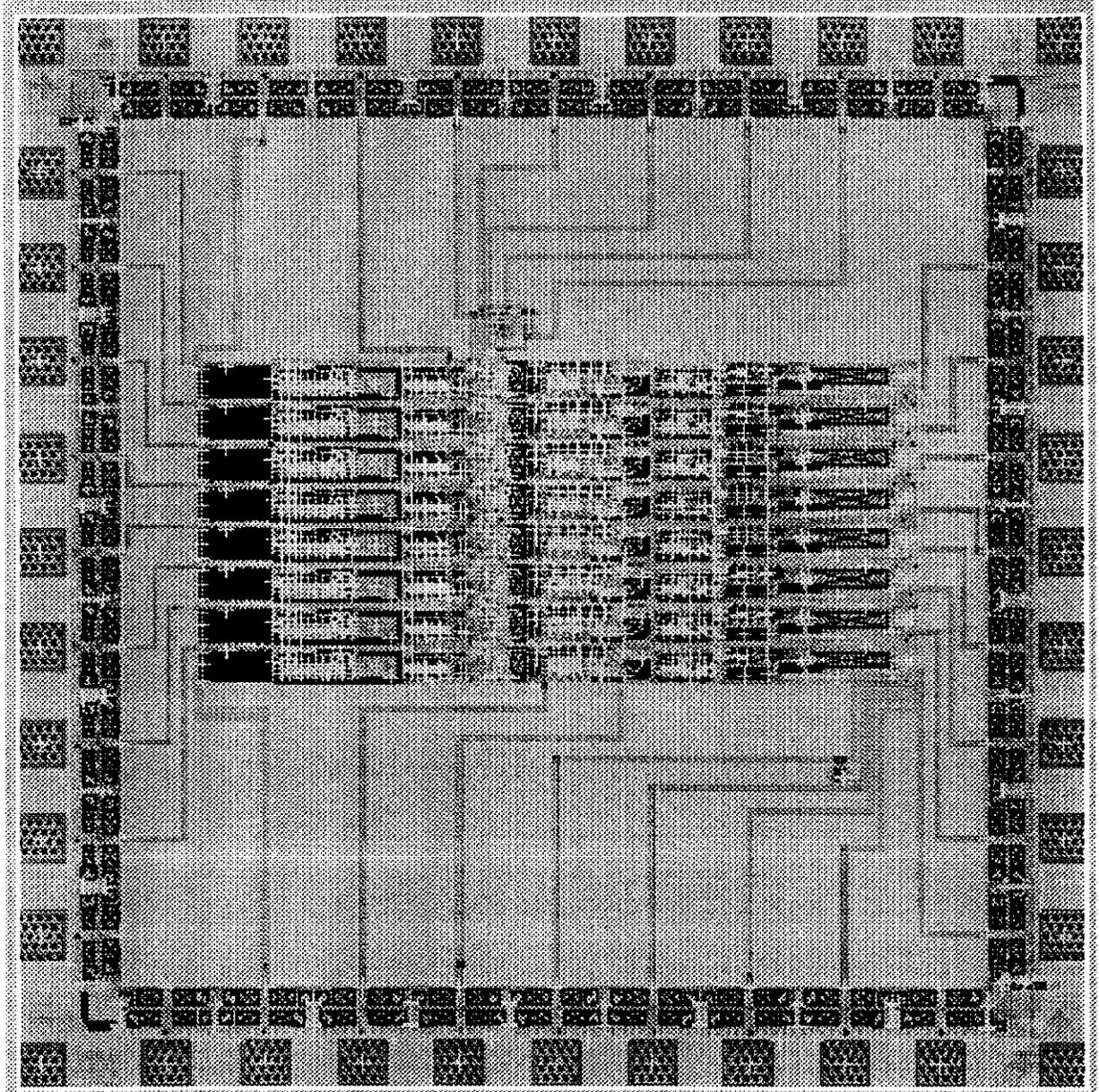
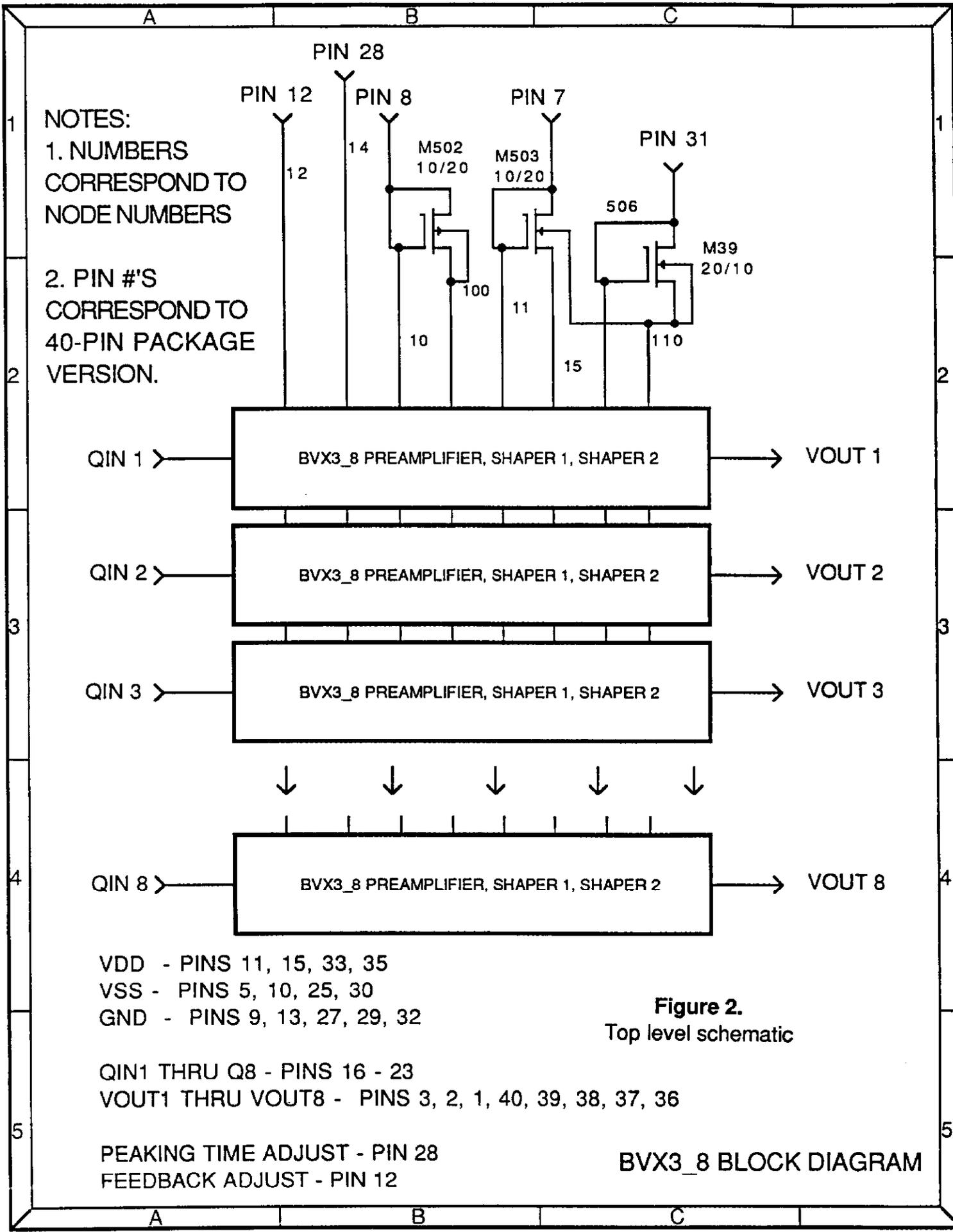


Figure 1.
Chip layout



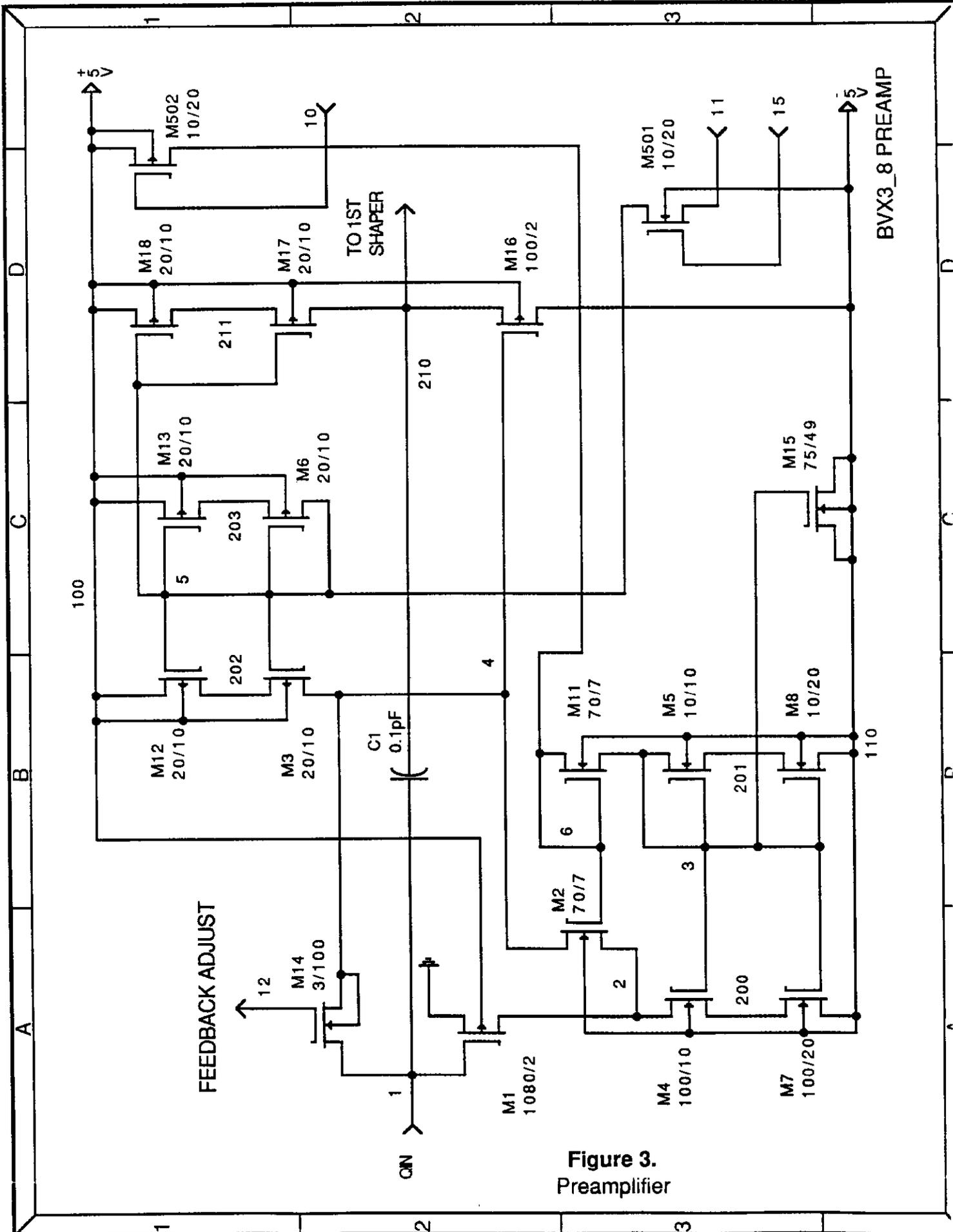


Figure 3.
Preamplifier

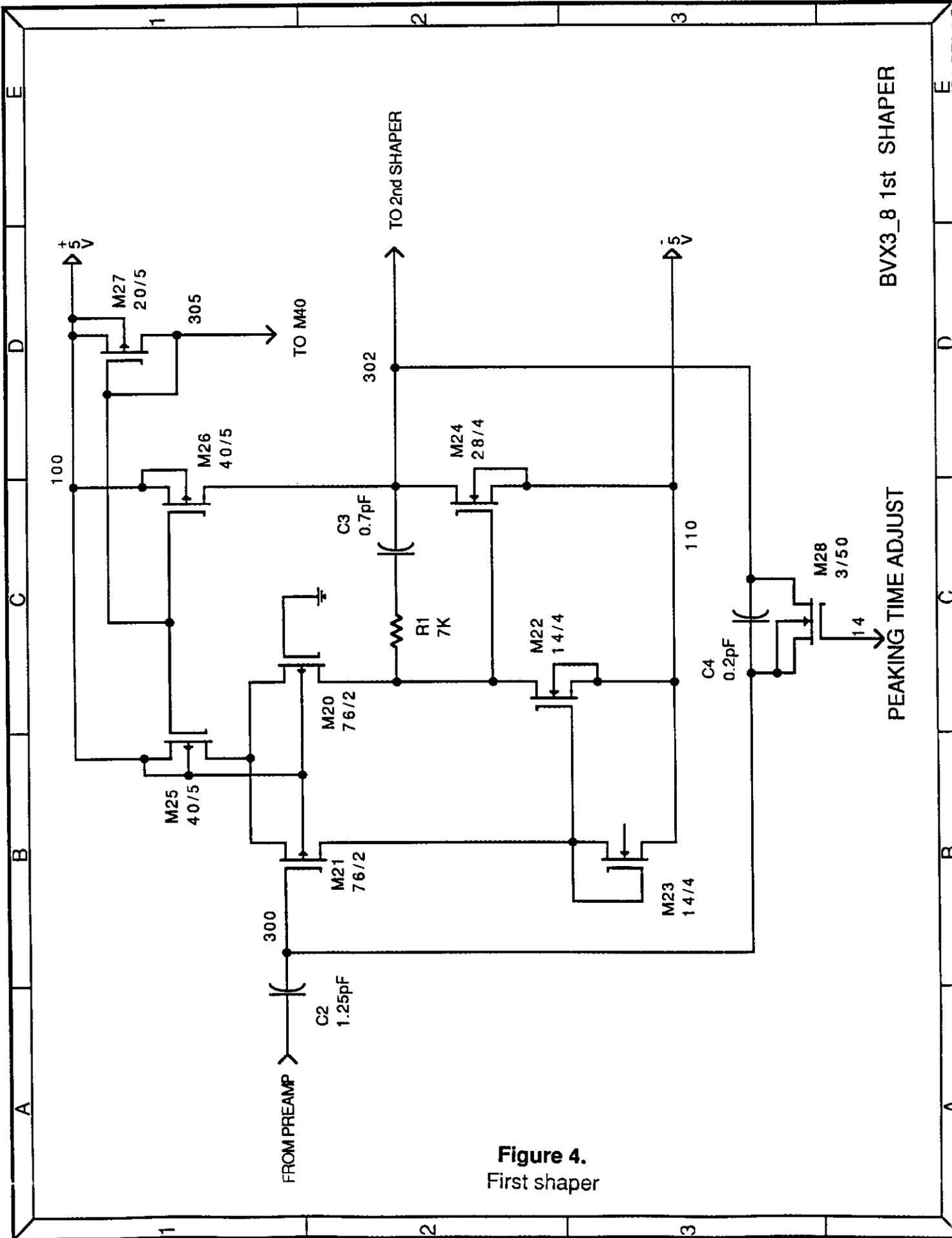


Figure 4.
First shaper

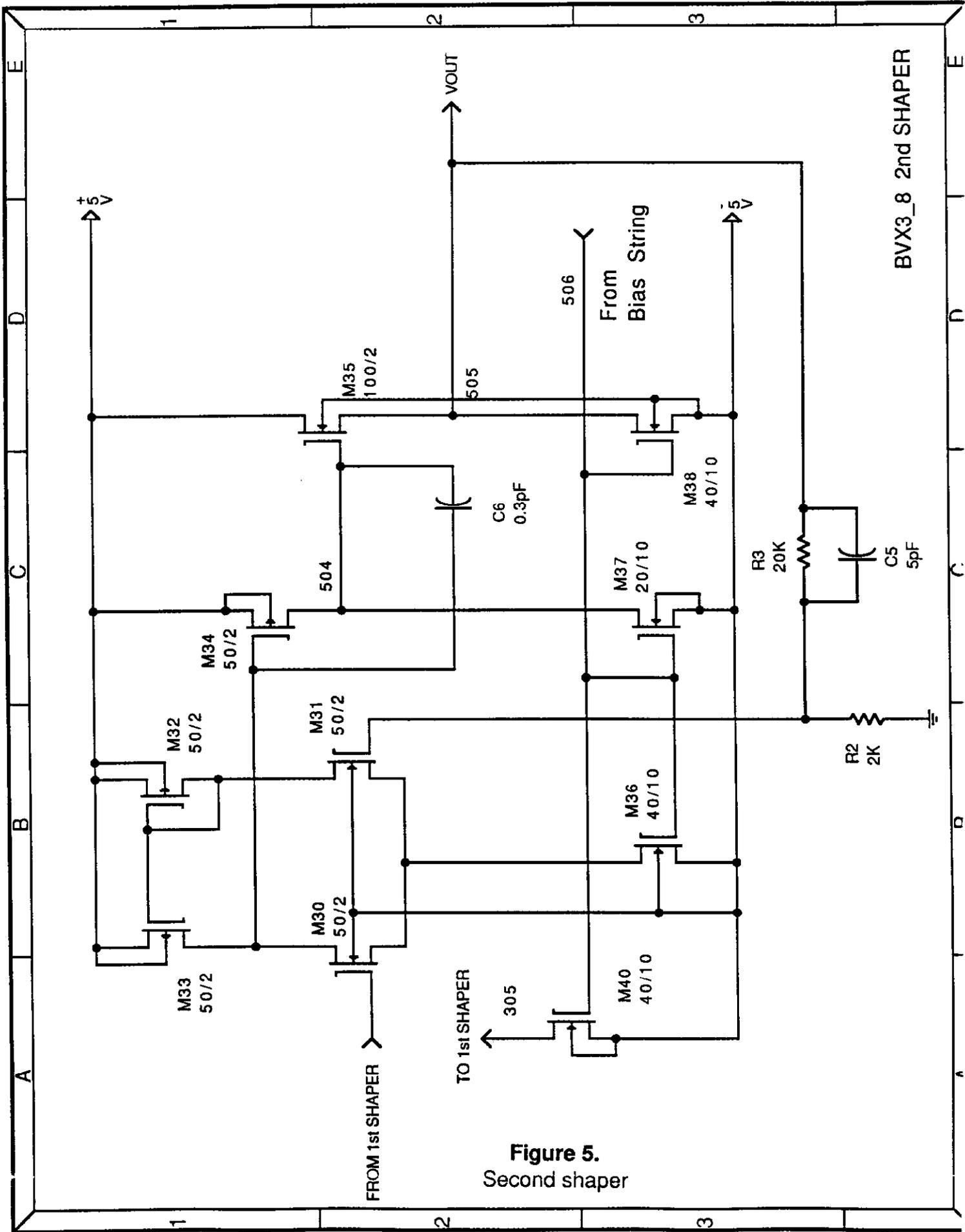


Figure 5.
Second shaper

BVX3_8 2nd SHAPER

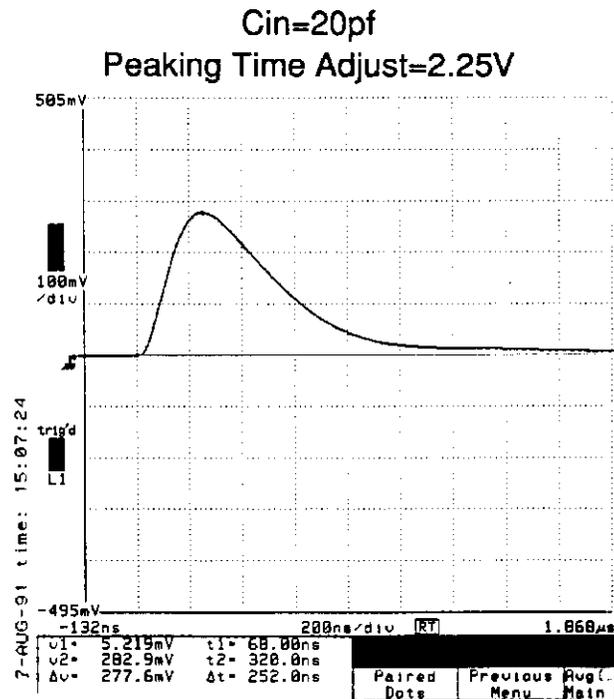
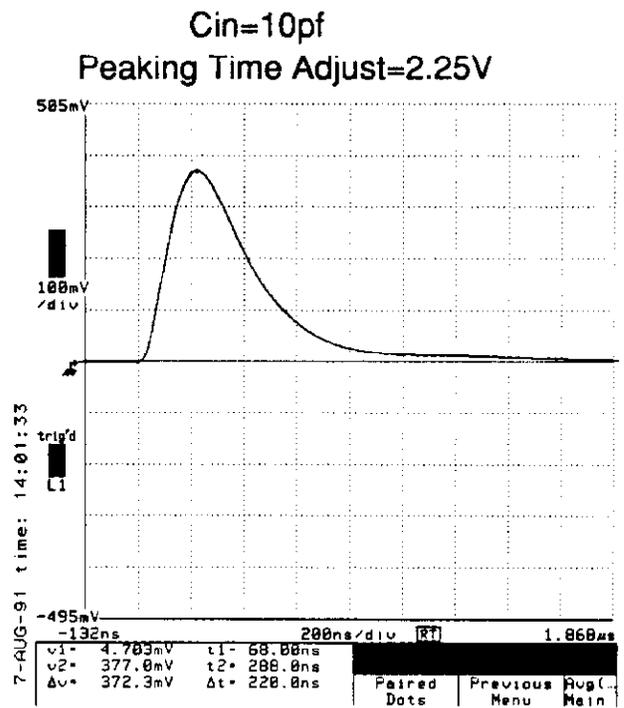
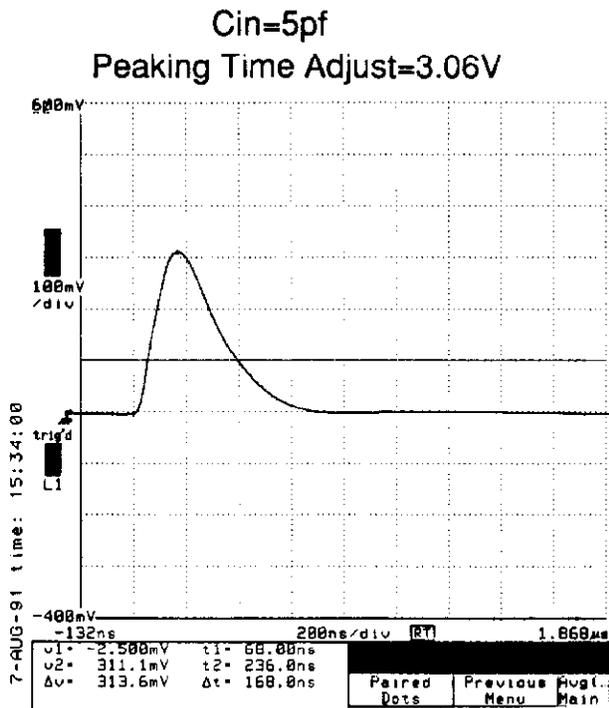


Figure 6.
Pulse Response vs. Input Capacitance (Qin=5fc)