national accelerator laboratory

TM-391
1105.31

PROPERTIES OF DIGITIZING CURRENT INTEGRATORS BUILT BY THE NAL RADIATION PHYSICS GROUP

R. Shafer

September 7, 1972

In conjunction with the construction of radiation monitoring equipment utilizing low current outputs of ion chambers and photomultipliers, we have designed and built a variety of current digitizers utilizing MOSfet and Jfet operational amplifiers with large dynamic range.

We have recently packaged one of these in a standard single width NIM module for general use, such as beam intensity monitoring using SEM's (secondary electron monitors) and I.C.'s (ion chambers). This unit was specifically designed to interface low current devices to scalers. The use of recently developed Jfets with low leakage has allowed the design of a unit with at least 2 decades higher digitizing rate than the commercially available units using MOSfets.

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Briefly the specifications are:

Polarity	negative current input
Leakage current	$\lesssim 10^{-12}$ amps
Digitizing calibration	10^{-10} Coul/pulse
Max digitizing rate	$>10^{5}$ Hz
Linearity; 10^{-10} amps $< I < 10^{-5}$ amps	$\pm 1\%$
Duty cycle limitations	none for $\lesssim 10^{-5}$ Coul in 1 second
Digital outputs	a) +5V pulse 1μ sec long into 50Ω
	b) $\overline{\text{TTL}}$ 1μ sec long into 100Ω pullup
	c) NIM fast 50n sec long into 50Ω
Estimated unit cost (parts & labor)	~$150.

In addition we have built MOSfet digitizers with leakage currents below 10^{-14} amps and a current range of 10^{-12} to 10^{-8} amps with a digitizing rate of $\sim 10^{-12}$ Coul/pulse and $\sim \pm 3\%$ linearity. However, no effort has been made to package this in a NIM module.

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CIRCUIT DESCRIPTION OF NIM CURRENT INTEGRATOR-DIGITIZER

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A circuit schematic of the digitizer described in TM-391 is shown in Fig. 1. An Analog Device #41J JFET op-amp is used in the summing junction mode as a current integrator. Integration is performed across a 1000 picofarad polystyrene capacitor. The circuitry connected to the (-) input has several functions. The 51 ohm series resistor acts as a termination for fast signals. The 1 μF capacitor and 100 k resistor act as a passive integrator to limit fast transients which may exceed the digitizing capability of the circuit. (Normally instantaneous current at summing junction should not exceed -10^{-5} amps.) These components may be changed as specific needs require. It should be noted that at large currents there is a voltage drop across the series resistor, which will affect the linearity if the input current source (sink actually) has an output impedance less than 10^7 ohms. The test button injects 1 nanoamp into the circuit for ascertaining the proper operation of the circuit. This circuit has a second function - balancing the input bias current offset: the 10^{10} ohm resistor allows the input voltage offset adjustment to vary the current through it in order to balance

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the total offset currents to zero. If the effective output impedance of the input current source is less than 10^{10} ohms, then this adjustment should be made with the input current source connected, but turned off. The adjustment is made by varying the 20 k pot and setting the dV/dt at the test point to less than 1 mv/sec.

A μA 734 precision voltage comparator is used with a small amount of hysteresis as a Schmitt trigger to detect the output voltage of the integrator. The comparator output is TTL compatible and drives a gated oscillator composed of two TTL integrated circuits. The output pulse widths of this circuit are determined by RC time constants in the multivibrators, and the circuit is specifically designed to put out square wave pulse trains in the event that the input current limitations of the integrator are exceeded.

Charge is pumped back into the summing junction via a pnp transistor circuit and a 2N4117A JFET. The JFET is used here rather than a regular diode as it has superior current leakage properties than available diodes, and is similar to the JFETS used on the 41J inputs.

Three output circuits are provided; a standard NIM fast signal (-1V into 50Ω, 30 nsec wide); a standard +5 volt signal (+5V into 50 ohms or greater, 1 μsec wide); and a TTL compatible signal (0 volts into a 50 ohm or greater pullup, 1 μsec wide).

No gating was included in the circuit, as it is extremely difficult to gate picoamp currents properly, and gating of digital signals is easily done at the scaler.

The entire circuit runs off of the ±12V supply of a NIM bin. The exact calibration of the circuit depends on the actual voltages so these should be measured and adjusted if necessary (use a DVM). It would have been more accurate to obtain a regulated ±15V by regulating the ±24V NIM supplies. In this case the only circuits which should be operated from the ±15 volt supplies are the 41J op-amp, the 734 comparator, and the pnp charge pump transistor.

A typical calibration is shown in Fig. 2. The major difficulty in calibrating the digitizer is locating accurate current supplies in the region of interest, as high-meg resistors have voltage and temperature coefficients, and change with age. (It should be noted that the calibration measurement was made with the 1 μF capacitor and the 100 k resistor removed from the input circuit for reasons already discussed.) The expected maximum leakage current is ±1 picoamp, and since no attempt is made to measure the actual voltage on the integrator, the lower limit to a total charge measurement over an interval of Δt seconds is

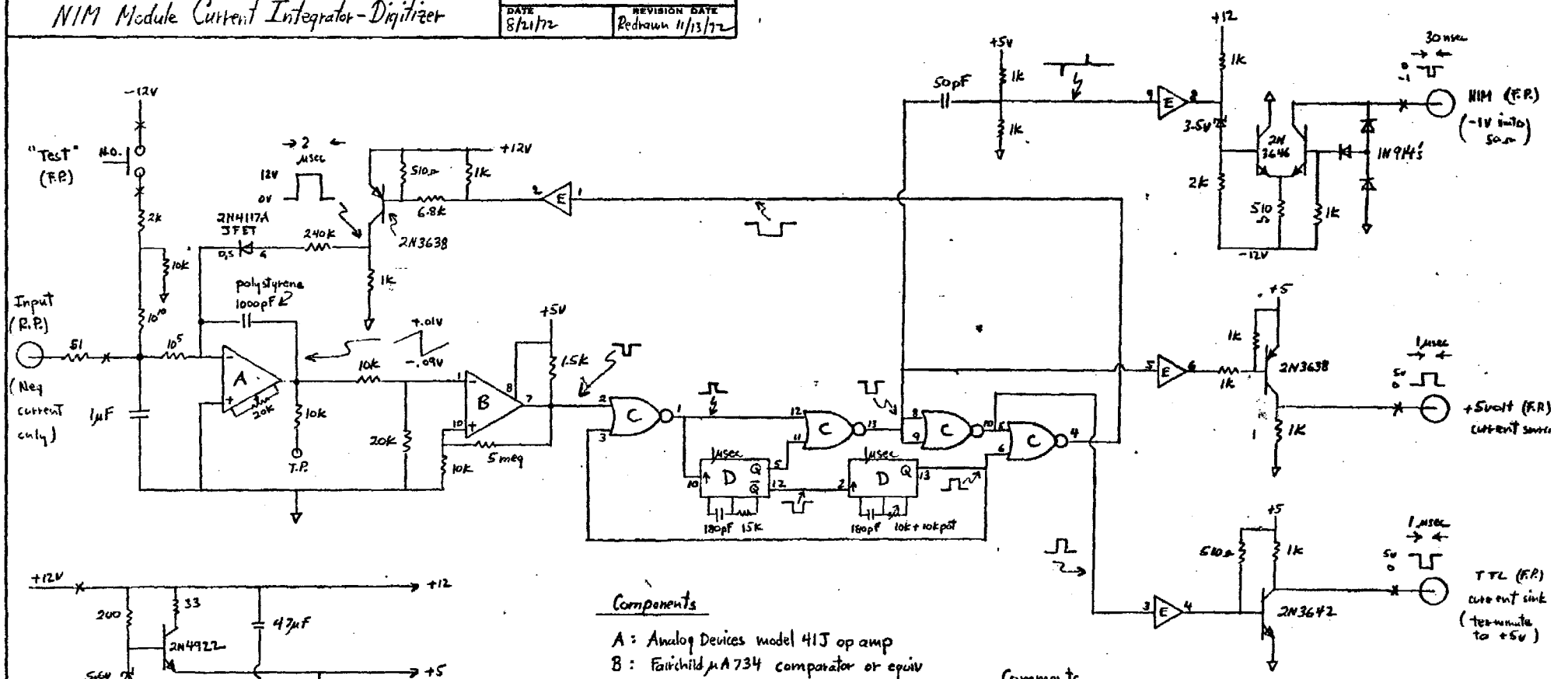
$$\Delta Q = \pm(1 + .01\ \Delta t) \times 10^{-10} \text{ Coulombs.}$$

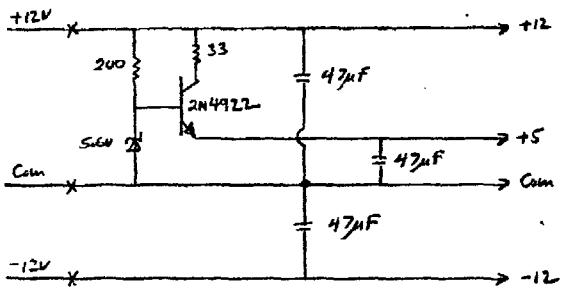
We have made this circuit operate at 10^{-11} Coul/pulse by changing the 240 k resistor in the feedback loop to 2.4 Meg, but this increases the time constant of the charge pump circuit and further limits the frequency at which the circuit can accurately digitize (to about 5×10^4 Hz or 5×10^{-7} amps).

Acknowledgment.

The author would like to thank L. Grumboski for his contribution in setting up and testing the prototype module, and laying out the art work for and fabricating the production units.

NATIONAL ACCELERATOR LABORATORY ENGINEERING NOTE	SECTION R.P.	PROJECT TM 391A	SERIAL-CATEGORY	PAGE Fig 1
SUBJECT: NIM Module Current Integrator-Digitizer	NAME: Shafer	DATE: 8/21/72	REVISION DATE: Redrawn 11/13/72	





Components

A: Analog Devices model 41J op amp
B: Fairchild μA 734 comparator or equiv
C: SN7402N Quad 2 input NOR gate
D: SN74123N Dual multivibrator
E: SN7407N Hex buffer

Notation

—x— Connection leaving p.c. board.
—o T.P. Test point
↑ Positive edge triggering
F.P. Front panel
R.P. Rear panel

Comments

1. With no input, adjust integrator output to minimum dV/dT using input voltage offset adj (1 pA leakage current ⇔ dV/dT = 10^{-3} V/sec)
2. For correct calibration, adjust 10k pot in gated osc.
3. Calibration unless otherwise specified is
   Hz output = -10^{10} I input ± 1% for $10^{-10} \le -I \le 10^{-5}$ amps
4. For best results, all connections to integrator (−) input should be guarded on both sides of p.c. board with guard ring attached to (+) input. Guard ring should be included in pc artwork.
5. Input 51Ω for fast signal termination. Input RC (1.0μF and 10^5) may be varied depending on characteristics of current input signal.
6. Calibration depends on exact voltage of ±12V supply. For better stability, regulate to ±15V from ±24V supply
7. For currents exceeding limitation of digitizer, the gated osc. circuit will put out a square wave signal ≈ 500kHz.

(cont)

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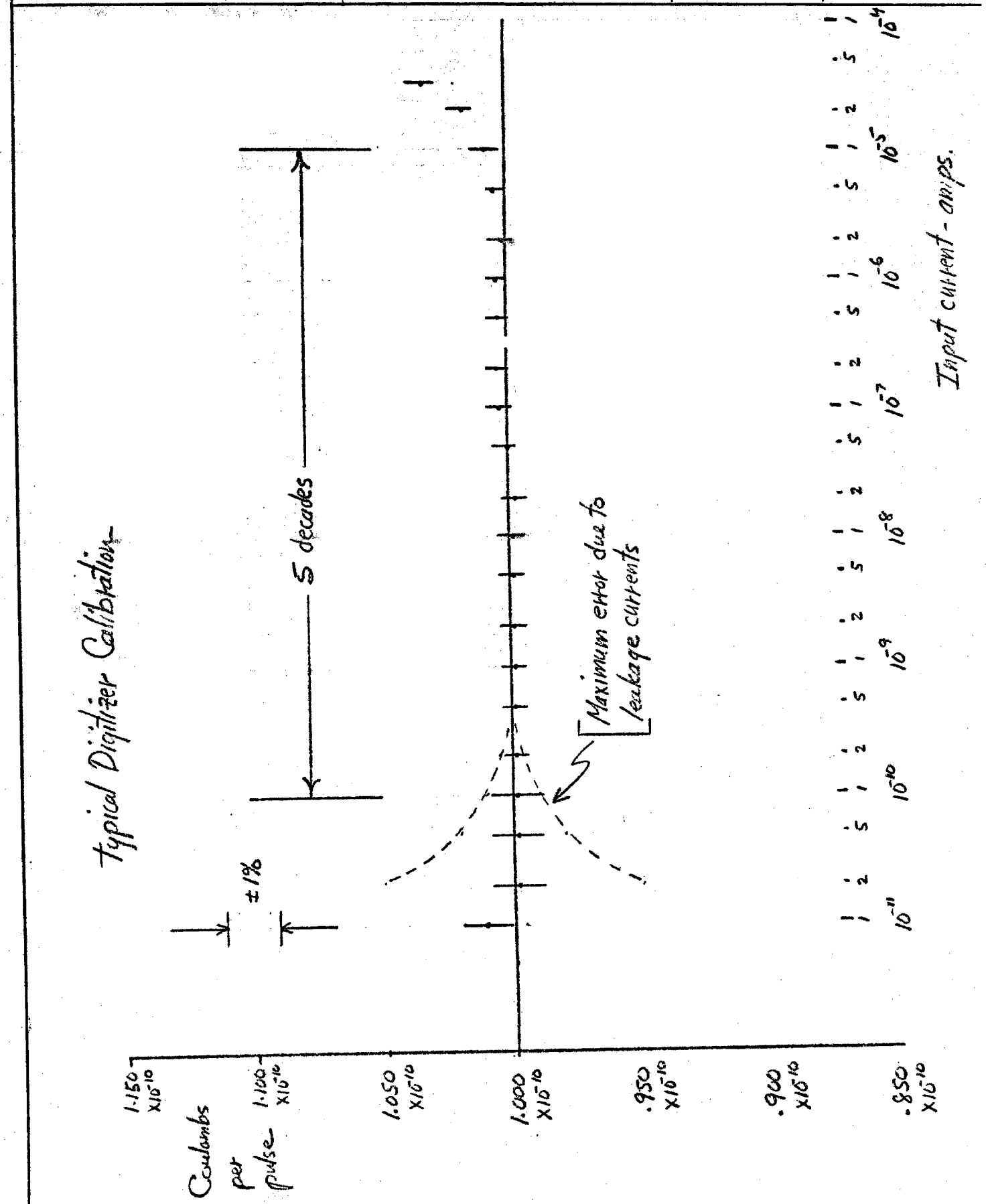
ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
	TM 391A		Fig 2

SUBJECT: NIM Module Current Integrator Digitizer - Calib

NAME: Shafer

DATE: 11/13/72

REVISION DATE: