



CURRENT STATUS OF LECROY 2280/2285 ADC SYSTEM

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ABSTRACT

The operating characteristics of the LeCroy Research Systems current version 2280/2285 ADC System (as modified at Fermilab for E516, E557, and E616) are reported. Work is proceeding at LeCroy Research Systems to improve many of these characteristics and the present versions are not viewed as fully developed.

Much of what has been learned during the development of these modules has been relevant to other components (e.g., the 2282 module) of the 2280 family. However, no testing of these other units has been carried out at Fermilab to date.

INTRODUCTION

The 2280 ADC System is a flexible, self calibrating, data sparsifying, high-sensitivity, linear, charge integrating ADC system. As such, it is a complex device with many characteristics to test. The present tests are not all-encompassing. On the other hand, they



relate to some of the more fundamental responses of the system in simulated experimental situations. The results relate to the following characteristics:

- a. Effective gate.
- b. Linearity of response to front panel inputs.
- c. Linearity of test pulse response and relationship to front panel response.
- d. Rate dependencies of pedestal and gain when the fast clear circuitry is used.
- e. Crosstalk from channel to channel.
- f. Noise rejection capabilities.
- g. Gain and pedestal dependencies.

These topics are treated one at a time in the following sections.

EQUIPMENT

The 2280 ADC systems tested were comprised of a system processor module (Model 2280) and individual 24 channel ADC modules (Module 2285), all housed in a single nonstandard CAMAC crate. The ADC modules make use of hybrid circuits (Model QD101A).

A list of modifications to the the originally delivered equipment is given in an appendix. Some of these modifications have been adopted by LeCroy in the versions leading to the current Mod 104. However, we list all the modifications since they may be of interest

to other users and since the standard production model has not yet been identified.

Test results are for fully modified modules only.

The tests were performed using standard NIM modules to generate gate and clear pulses and commercially available programmable digital delay generators and programmable DAC's to control gain and test level references. The various pieces of equipment were tied to a CROMEMCO microprocessor based system which allowed computer control, immediate information turnaround and hard copy outputs. All of this equipment was set up in the Instrumentation Evaluation Group of Research Services at Fermilab.

EFFECTIVE GATES

Using an external pulser it was possible to vary the relative times of the input and gate. In principle, one would like to move instantly from a period when no input signal is integrated to a time when all the signal is integrated. Figure 1 shows a plot of the integrated signal digitization for a 6 nsec wide logic signal applied at various times with respect to the gate. Four features are of interest. First, the turn-on time for the gate circuit is about 15 nanoseconds as is the turn-off time. Channel to channel variation of effective gate width is about 5 nsec. Second, the effective gate turn-on time varies from channel to channel by up to 10 nsec relative

When consistent with experimental application, removed the fast clear operation completely. In this case, every gated event is read out.

Additional modifications for clearing at proper times as when F9 or C CAMAC commands are received.

Adjust wait monostable before conversion started to match experiment needs related to noise and pedestal values.

to the appropriate front panel input. Third, there is a 10% variation of gain across the 75 ns plateau (full acceptance) for a 100 ns applied gate. Finally, there is a gross non-linearity of the ADC response during the turn-on of the gate circuit. Figure 2 shows the size of this effect. The gain is a function of the applied charge or voltage!

LINEARITY OF RESPONSE TO FRONT END INPUTS

One of the most impressive features of these ADC modules is the linearity of response in the middle region of the gate period over a very wide dynamic range. Table I contains the results of fits to the response to charge applied to the input for a variety of gains and full scale values. All tests were performed using an applied gate of 150 nsec and a charge pulse of 10 nsec rise time and 40 nsec fall time. Special care was taken to insure that the pulse started well after the gate became effective.

The results are shown in Figure 3 where the deviations from the $\text{Response} = (\text{gain} * \text{charge} + \text{pedestal})$ fits for 24 channels in one module are shown. The rms deviation of the response to a linear fit was typically less than a count. Individual values are listed in Table I.

TEST PULSE RESPONSE

Because of the charging time of the test pulse circuit (10 microseconds) and the amount of charge required for a large system, it is inappropriate to enable the test pulse circuit during normal data taking for many experiments. In this case, the pedestal value (response for no input charge) is different between normal data and test pulse enabled data. However, the test pulse measured gain and nonlinearity is found to be representative of the front panel response for these features. Table II shows the response to test pulse operation akin to the results of Table I with a front panel input to the same channel. The final column gives the ratio of linear fit coefficients in the two tests. Using only one normalization point, this ratio is 1, typically within 0.5%. This demonstrates how well the test pulse data represents the front panel response.

Although the above results are very impressive, they are not characteristic for the unaltered module. They are characteristic only when both the front panel and test pulse inputs arrive in the middle period of the effective gate. Those channels closest to the front panel show particularly large deviations from the above ideal. The timing of the gate induced test pulse is neither uniform nor optimized. Early tests when the present circuit was adopted showed the need to keep the input signal in appropriate time relation to the gate.

RATE DEPENDENCES

Two separate tests of rate effects have been conducted. One, referred to as the "pump-up" test, imposed repeated alternate gates and fast clears until a final gate was followed by readout without a fast clear. The pedestal was monitored as a function of the number of gate-clears before a readout. The pulses received by the processor are indicated in Figure 4a. The second test, referred to as the "simple rate" test, systematically changed the time between a readout and the previous clear. The pulses received by the processor are indicated in Figure 4b. In this test, two gate signals are received for each readout, a first with a fast clear quickly following and then a second after a predetermined time for readout. In both tests, the time required for a readout was long and small variations of its length were ignored.

The results of these tests (Figure 5) indicate two strong rate dependences, each on the order of $\pm 1/2$ picocoulomb. This may be many counts for the sensitive gain settings of which the device is capable. The effect is to reduce the maximum useful sensitivity for experiments with random event occurrences.

Using the external charge pulser and putting a known charge into the ADC channel during the last gate of Figure 4a, it was possible to measure the sensitivity of the module under differing event rates. No

reproducible gain changes of more than 1% were observed as a function of gating rate.

CROSSTALK

The feedthrough of signal from one channel to another on the same board varies from about 40 to 60 db. That is, channels which are adjacent and share the same test pulser input cable have about 1% feedthrough of signals. Other channels are typically a factor of ten better isolated. These effects include those due to the five foot long multicoaxial cables we used to get the signals into the multiconductor input connector.

NOISE REJECTION CAPABILITIES

The inputs of each channel are quasidifferential. In addition, the layout on the printed circuit board is such that the chassis ground is isolated by a 1K ohm resistor per board and 0.022 pfarad capacitors per channel. These features make suppression of ground loops a function of other system elements. A series of tests were performed to determine the effects of positive and negative voltages up to 0.5 volts d.c. and 0.2 volts peak to peak 60 and 120 herz applied between the input signal return and ground. No broadening of the distribution of pedestal values for a series of readings was observed. However, the average pedestal value does depend on these levels. In this context, it should be observed that the rms width of

a typical pedestal distribution is about 15 femtocoulombs with no cables plugged into the front. In two setups in running experiments, the rms pedestal width has increased to about 40 femtocoulombs. Of course, both experiments have required special care (using quite different techniques) to achieve these values. One low rate experiment uses a.c. coupling and shorts out the 1K ohm resistor on each board. The other uses d.c. coupling and no short. These widths are achieved only when the rate dependence of the pedestal is absent.

GAIN AND PEDESTAL DEPENDENCIES

The gain of the ADC modules can be controlled by using an external reference rather than the internal one. The gain and pedestal dependence of a typical channel are shown as a function of this reference for a 150 nsec gate in Figure 6. This data is for a WAIT monostable of 3 usec as supplied with the unit. The pedestal dependence on gate width is shown for another channel in Figure 7. Increasing the WAIT time (before digital conversion) can be used to reduce apparent pedestal values. However, the "pump up" effect is significantly worsened by this procedure.

ACKNOWLEDGEMENT

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APPENDIX

MODIFICATIONS MADE SO FAR DURING DEVELOPMENT

STAGES OF LECROY 2280/2285

The items in the following list are arranged by category - i.e., according to the purpose for which they were intended. The bulk of these items were worked out at Fermilab, with the knowledge of LeCroy Research Systems. Most are expected to be retained for the final standard units as delivered by the manufacturer.

Poor linearity after early fix for worst rate dependences.

Changed pedestal compensation pin on hybrid from floated to +9 volts.

Correction of crate loading problem when more than one module is in the crate.

Isolation of the sensitive +6 volt power from the +5.2 volt burst loaded power.

Addition of external +6 volt power on the Y2 and G CAMAC bus lines.

Protection Ge diodes added to prevent damage when CAMAC and external supply not both on or off.

Smooth response of linear gate circuit.

Remove C5 capacitor.

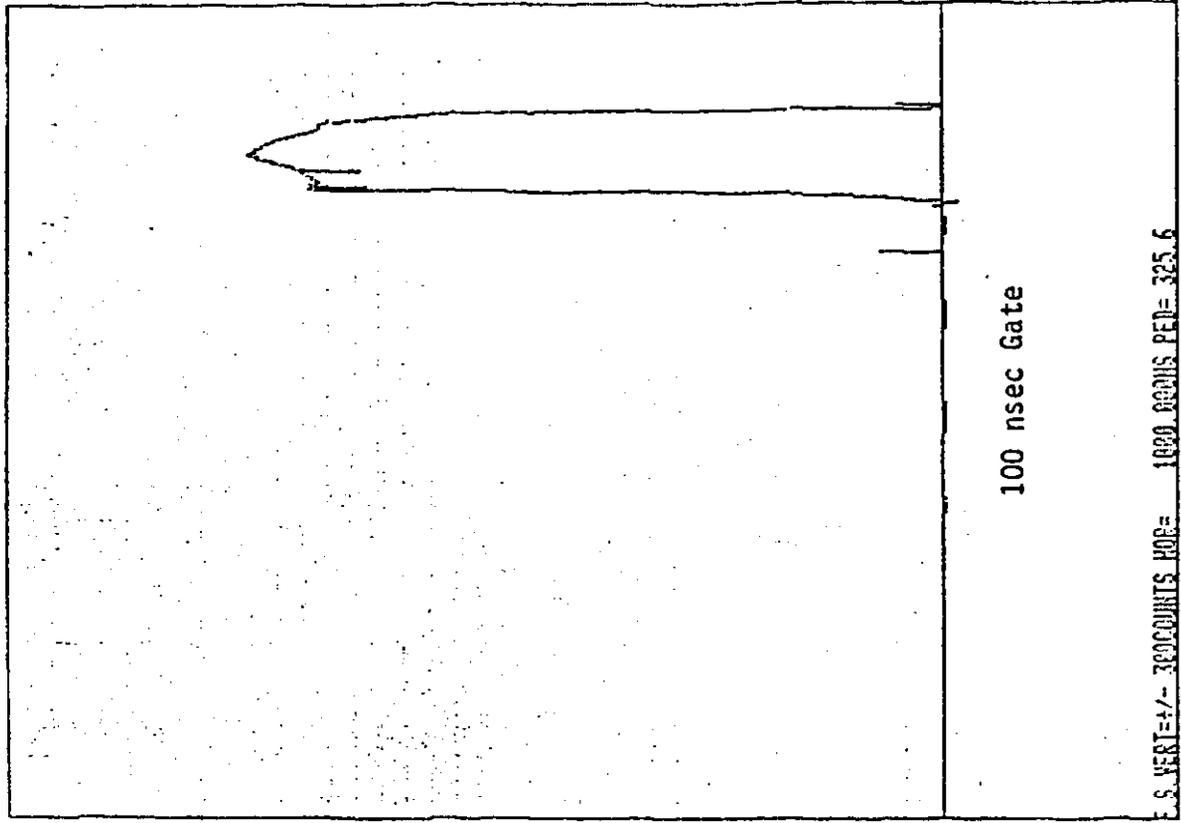
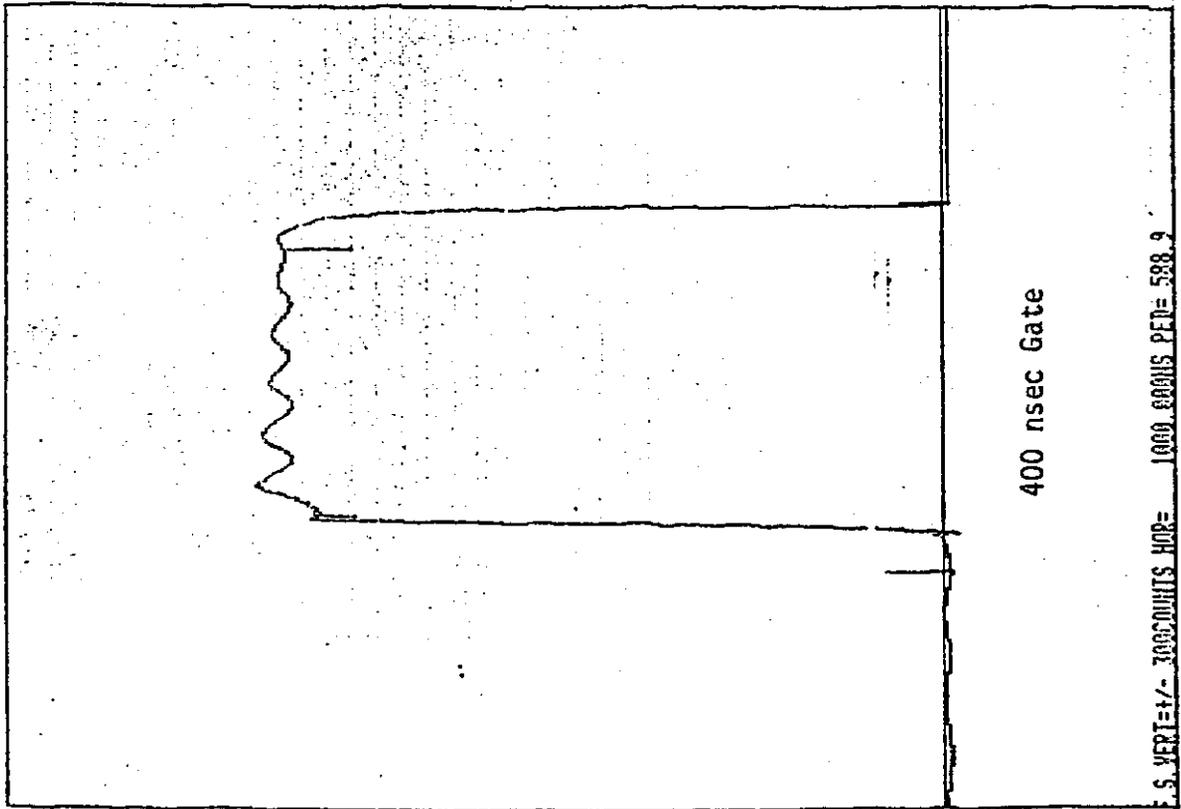


Fig. 1 Moving

inal Through Gate

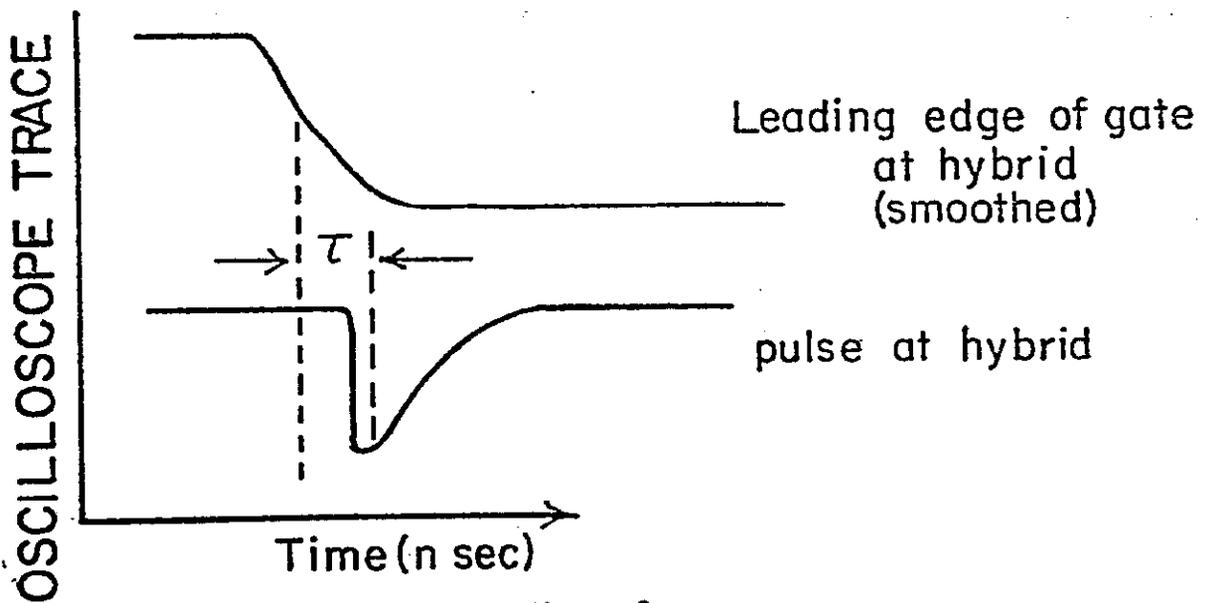
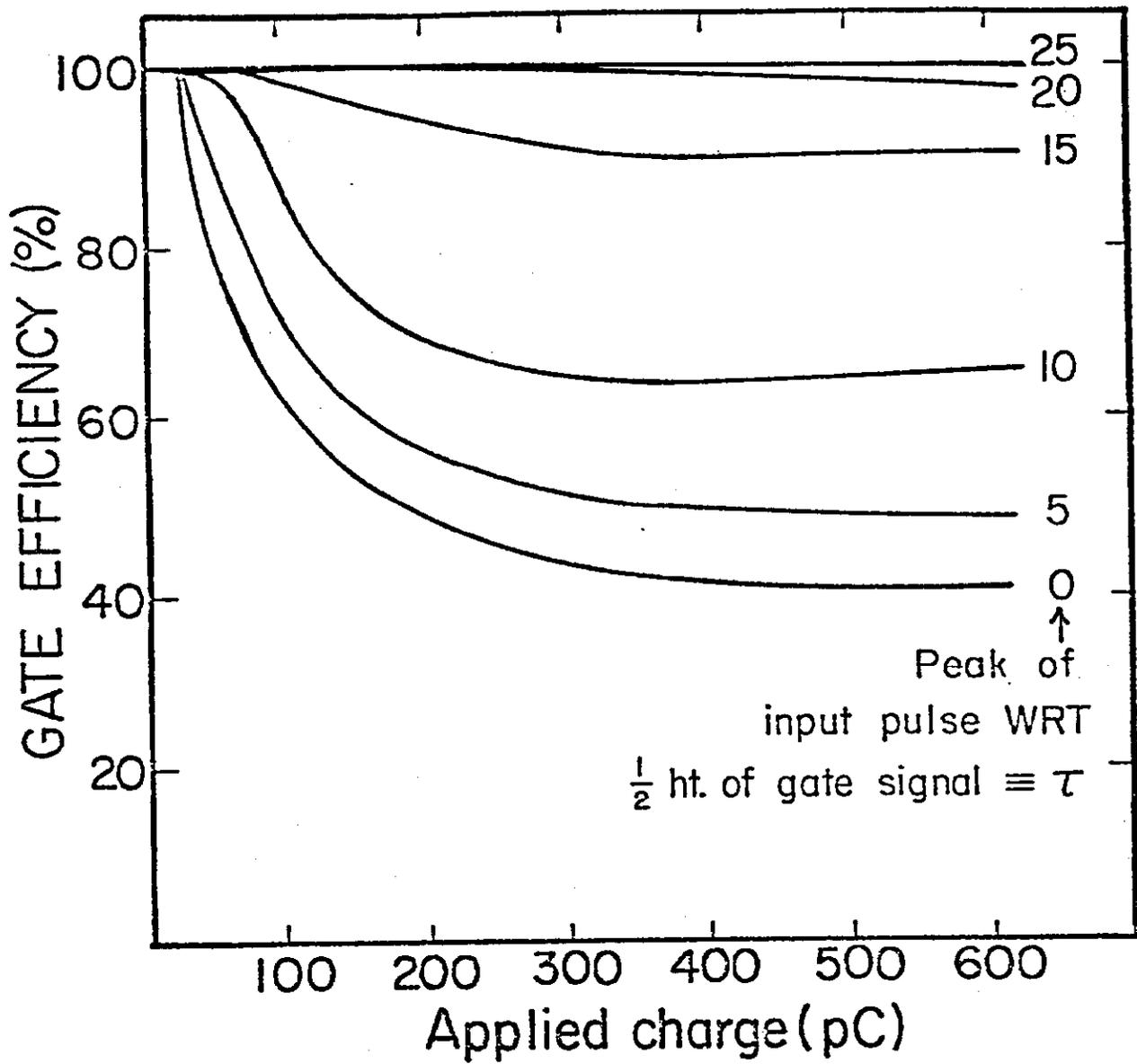


Figure 2

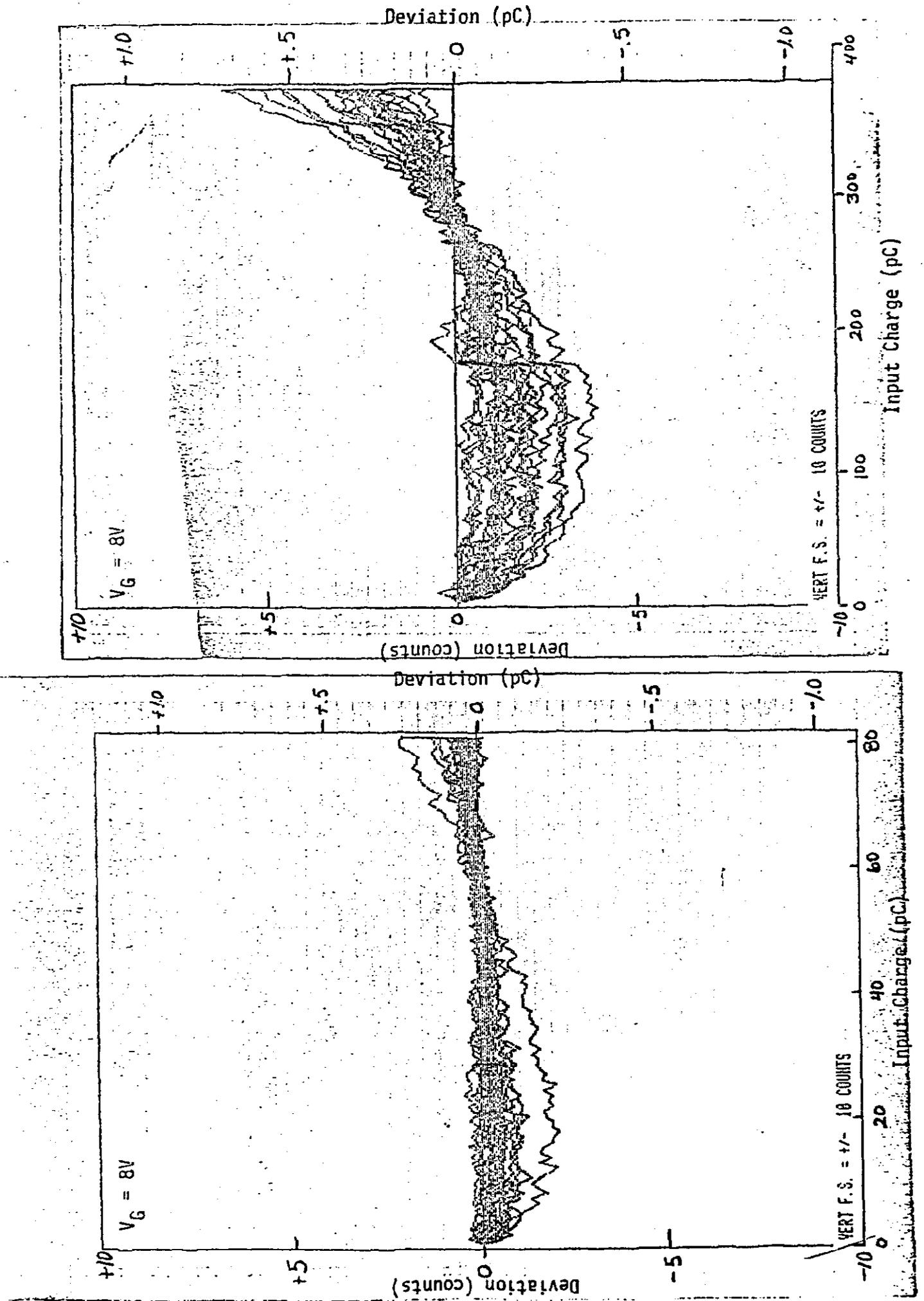
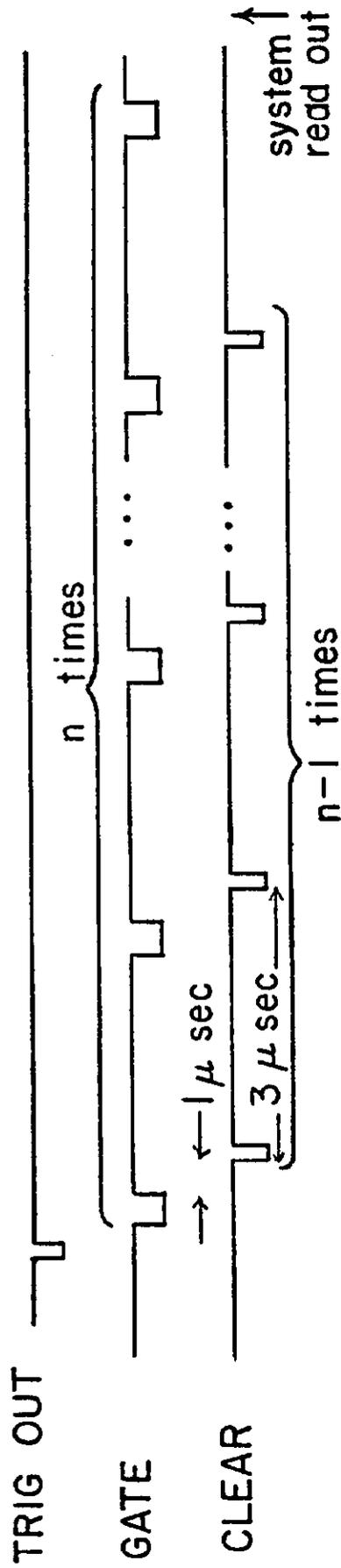
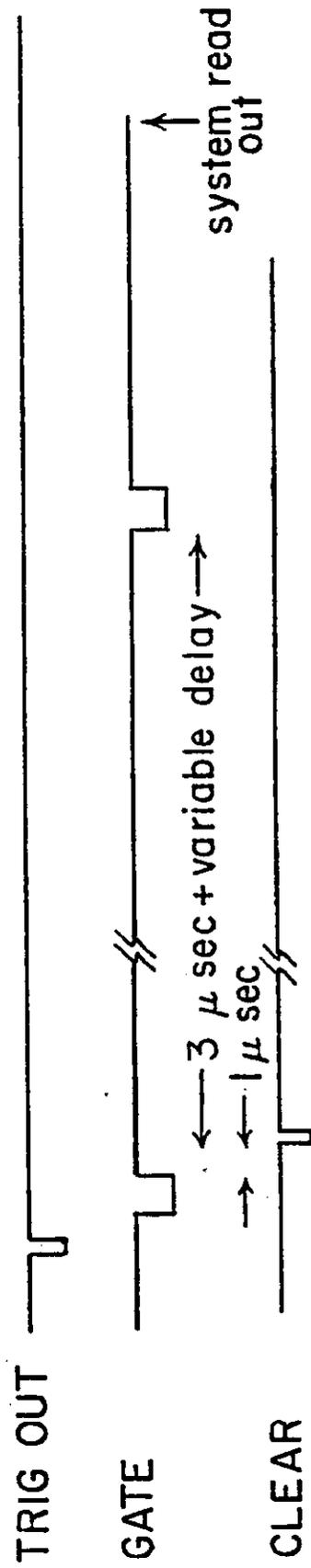


Figure 3 Deviation From Linear Fit



"PUMP UP" TEST SIGNALS

Figure 4a



"SIMPLE RATE" TEST SIGNALS

Figure 4b

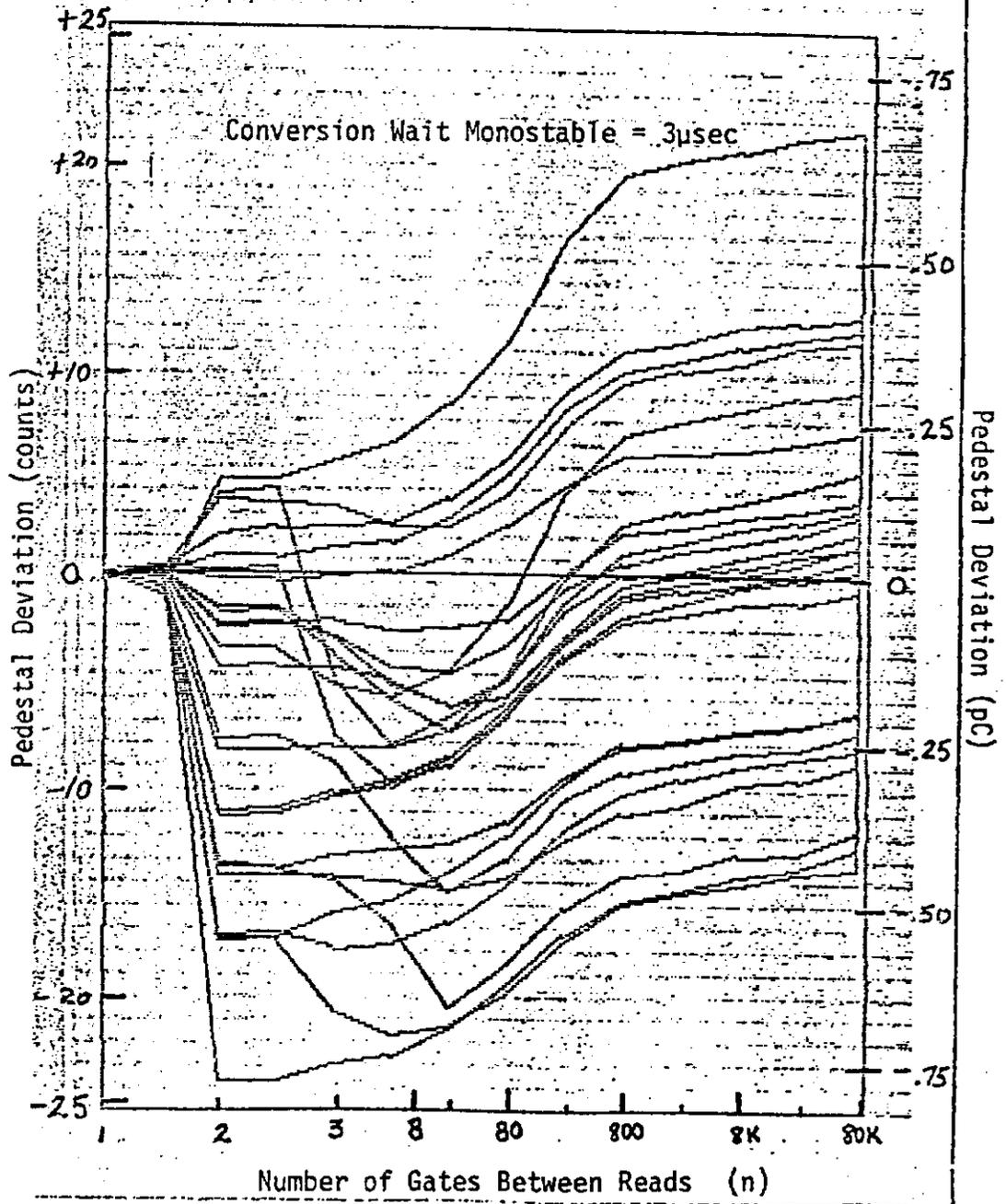


Fig. 5a. Pump Up Effect

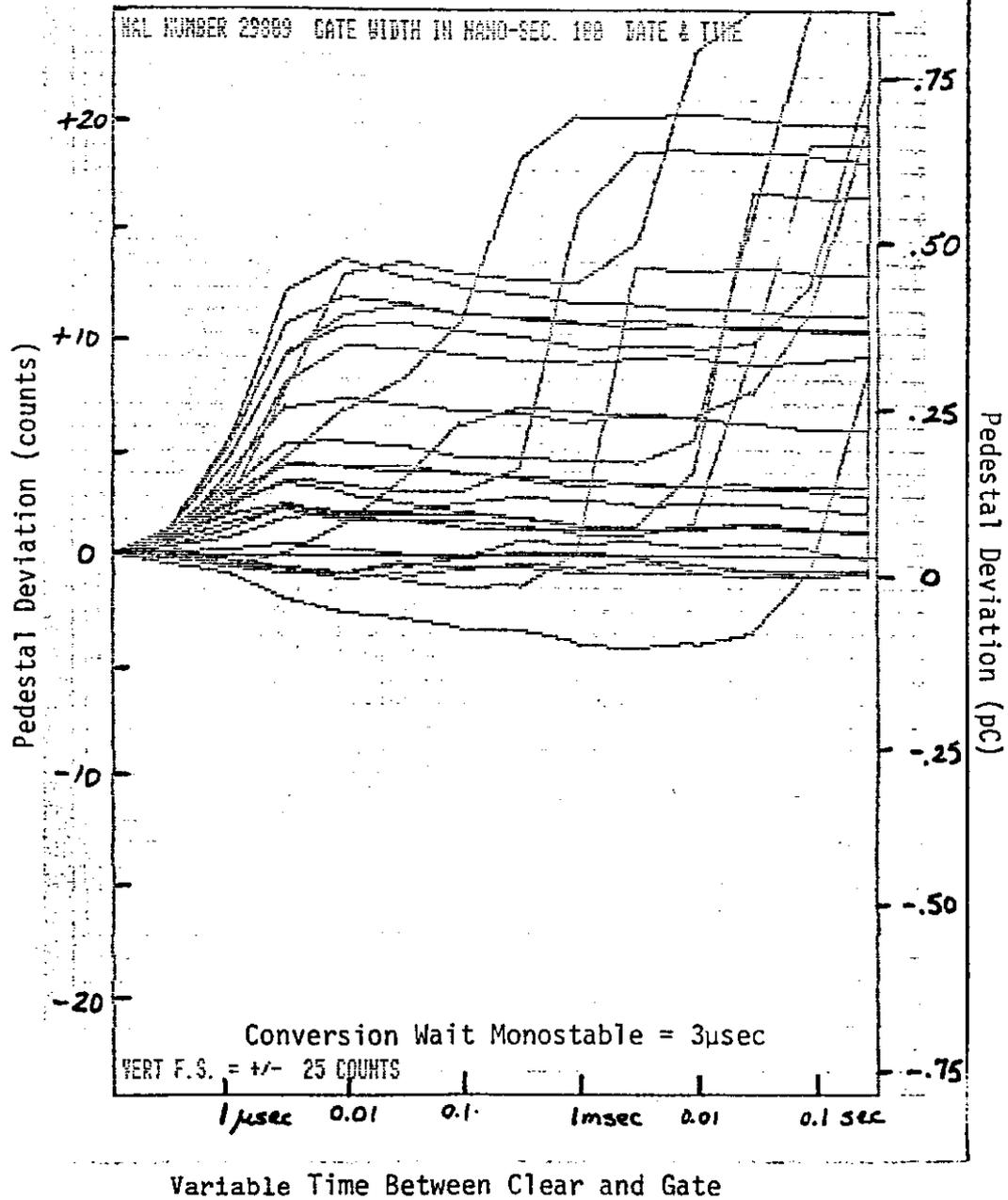


Fig. 5b. Rate Effect

TABLE I

RESPONSE TO FRONT PANEL INPUT

Gain Reference (Volts)	Approximate Maximum Charge Used In Fit (pC)	Pedestal (Counts)	Gain, m Response=mQ (counts/pC)	Avg. rms Deviation from Fit (counts)
1.0	.4	2592	60.9	.2
	8	2592	61.2	.2
2.0	4	1204	31.2	.6
	8	1204	31.4	.5
	20	1204	31.7	1.0
	40	1204	31.8	1.2
	80	1204	31.8	1.2
4.0	4	502	16.5	.2
	20	502	16.6	.3
	40	502	16.6	.5
	200	502	16.7	.5
8.0	4	138	8.7	.3
	20	138	8.9	.2
	40	138	8.9	.1
	200	138	8.9	.3
	400	138	8.9	1.3

TABLE II

RESPONSE TO INTERNAL TEST PULSER

Gain Reference (Volts)	Approximate Maximum Charge Used In Fit (μC)	Pedestal (Counts)	Gain, m Response= mQ (counts/ μC)**	Avg rms Deviation From Fit (counts)	m_{Internal} $m_{\text{Front P}}$
1.0	4	2635	60.4	.7	.992
	8	2635	61.0	.7	.997
2.0	4	1225	31.4	.3	1.005
	8	1225	31.4	.5	1.000
	20	1225	31.6	.6	.997
	40	1225	31.6	.8	.996
	80	1225	31.7	1.0	.996
4.0	4	513	16.5	.3	1.000
	20	513	16.6	.3	1.000
	40	513	16.6	.4	1.000
	200	513	16.7*	.9	1.000*
8.0	4	144	8.9	.2	1.014
	20	144	8.9	.3	.999
	40	144	8.9	.2	1.003
	200	144	8.9	.3	1.002
	400	144	8.9	.3	1.001

** Normalized at * to agree with Table I.