



# Measurement of the single event upset cross section in the SVX IIe chip

A. Juste

*Fermi National Accelerator Laboratory, Batavia, Illinois 60510*

S.M. Tripathi

*University of California, Davis, California 95616*

D.A. Wijngaarden \*

*University of Nijmegen, 6525 ED Nijmegen, The Netherlands*

---

## Abstract

The Single Event Effect cross-section for the SVX IIe readout chip has been measured using 63.3 MeV protons from the UC Davis cyclotron. The expected rate of Single Event Upsets in the DØ Silicon Microstrip Tracker, which uses the SVX IIe chip, is low enough for stable running. No Single Event Latchups were recorded. The chips withstood radiation doses of over 3 Mrad ( $3 \times 10^4$  Gy), well over the dose expected for the anticipated exposure of the detector.

*Key words:* single event upset, radiation tolerance, silicon detector

*PACS:* 85.40.Qx, 29.40.Gx, 29.40.Wk

---

---

\* Corresponding author.

*Email address:* [dwijngaa@hef.kun.nl](mailto:dwijngaa@hef.kun.nl) (D.A. Wijngaarden).

## 1 Introduction

Run 2 of the upgraded Tevatron collider at Fermilab started in March 2001. The accelerator goal for the first phase of Run 2 is to deliver an integrated luminosity of 2-4 fb<sup>-1</sup> by 2005. The DØ detector at Fermilab has been upgraded in order to fully exploit the physics opportunities of this run [1]. One of the most important aspects of the upgrade is the replacement of the inner tracking system with a 792,576 channel Silicon Microstrip Tracker (SMT) [2] and a scintillating fiber tracker, both embedded in a 2 Tesla axial magnetic field. The SMT has been designed specifically for the first phase of Run 2.

The signals from the SMT are amplified and digitized by the SVX IIe chip [3]. The SVX IIe chips are mounted on hybrids, which are glued to the silicon sensors with each preamplifier input wirebonded to a silicon strip. A hybrid is a kapton-based flexible circuit laminated on a beryllium plate, containing only the chips and passive electronics. It provides routing of the signals to and from the readout system. The basic readout unit of the SMT is a hybrid containing 3, 6, 8 or 9 daisy-chained chips. There are 6092 SVX IIe chips in the SMT, located at radii ranging from 2.7 cm to 25 cm. The intense flux of hadrons to which the chips will be exposed raises concern that the operation of the SMT may be affected by Single Event Effects (SEE).

SEEs occur in micro-electronic circuits through energy deposition of heavy ions in a small sensitive volume of an integrated circuit. They can be destructive (hard) errors like single event latchups or static (soft) errors like single event upsets.

A Single Event Upset (SEU) is a change of the value of a memory cell due to radiation-induced charge collection at the nodes of the cell. SEUs can interrupt logic functions of a chip, but they can typically be recovered by cycling power or rewriting the data.

A Single Event Latchup (SEL) is due to radiation-induced turn-on of parasitic transistors in a CMOS chip. When latch-up occurs, the chip symptomatically draws a large current and may fail if power is not turned off quickly. No SELs were recorded during the test. The remainder of this article will focus on Single Event Upsets.

To test the SEE sensitivity of the SVX IIe chips, the SEE cross section for these chips has been measured at various angles of incidence with 63.3 MeV protons at the UC Davis cyclotron [4].

The tests at the UC Davis Cyclotron are the only high dose (> 2 Mrad) exposure tests performed with the SVX IIe chips to date. A short discussion of the integrated dose performance of the chips is included.

## 1.1 Single Event Upset Phenomenology

### 1.1.1 Dependence on device specifications

The Single Event Upset rate depends on the energy, type and angle of incidence of the incident particle and on the threshold energy and sensitive area of the device. The threshold energy needed to cause an upset depends on the design and technology of the circuit. As the minimum charge collection needed is proportional to the node capacitance and the supply voltage, SEU sensitivity is expected to increase with smaller feature size [5].

### 1.1.2 SEU cross section for different particle types

The ionization energy of nucleons and charged hadrons is typically too low to cause upsets in CMOS components. Upsets from such particles are caused by heavy ion fragments from a nuclear interaction of the incident particle in the silicon. The hadronic radiation background at the Tevatron primarily consists of protons, neutrons and charged hadrons (mostly pions). Huhtinen and Faccio [6] show that for energies above 20 MeV the cross sections for neutrons and protons are almost identical. The upset rate for pions at high energies (200 MeV) is twice that of protons of the same energy. They also argue that for low energies ( $< 3$  MeV) the upset rate for neutrons is negligible in a typical accelerator environment and for most components. The measurement of the SEU cross section for protons at 63 MeV will be used to estimate the expected rates at DØ.

### 1.1.3 SEU cross section for different particle energies

As a function of incident proton kinetic energy, the SEU cross section rises rapidly from threshold and asymptotically approaches a limiting value at high energy. The semi-empirical two-parameter Bendel model [7] can be used to describe the incident proton energy ( $E$ ) dependence of the SEU cross section for devices with small feature size (in upsets per proton/cm<sup>2</sup> per bit):

$$\sigma(E) = (B/A)^{14} [1 - \exp(-0.18Y^{0.5})]^4$$

where

$$Y = (18/A)^{0.5} \times (E - A),$$

and  $(B/A)^{14}$  is the asymptotic cross section  $\sigma_\infty$ . Here,  $A$  is the proton energy needed for upset or threshold energy, and  $B$  is a constant to be determined

from the limiting cross section. With only one measurement at a given energy  $E$ , it is customary to use a one-parameter Bendel model, with  $B = 24$ , to extract the threshold energy  $A$ . The Bendel curves, normalized to  $\sigma_\infty$ , for four values of  $A$  are shown in Fig. 1. Unfortunately, the one-parameter Bendel model can not simultaneously describe the threshold and the asymptotic cross-section regions [8], leading to a significant over-estimate of the asymptotic cross-section if  $A$  is determined from nearby the threshold.

#### *1.1.4 SEU cross section and angle of incidence*

Monte Carlo studies of energy deposition show that for devices with small lateral dimensions, small sensitive layer thickness and high threshold energies, the SEU cross sections may be significantly higher at large angles of incidence of the proton [9,10]. An angular dependence has also been measured for the SVX3 chip by the CDF collaboration [11]. We will use our measurement at large angles of incidence to provide a conservative estimate of the SEU rate for the SMT at DØ.

### *1.2 SVX IIe Chip*

The SVX II chip is the third generation of the original SVX chip [12]. It contains both analog and digital sections on a single die. It was designed in  $1.2 \mu\text{m}$  UTMC technology for radiation hardness. The operating voltage is 5.0 V.

Each chip contains 128 readout channels of identical electronics (preamplifier, pipeline and ADC) along with digital circuits common to all channels. Charge collected by a silicon strip on the sensor is received via a bond pad and integrated in the preamplifier. A 32 cell deep analog pipeline sequentially samples the output of the preamplifier at a rate given by the bunch crossing frequency (maximally 7 MHz) and stores the charge pending an accept signal. The integrated charge of the selected bunch crossing is digitized in an 8-bit Wilkinson-type ADC at 106 MHz. Sparsification logic is available on the chip.

To optimize performance, the SVX IIe chip has many programmable features including test input channel mask bits, preamplifier bandwidth, pipeline depth and ADC gain. Control parameters and channel masks can be set during initialization through a 190-bit serial shift register. Of these 190 bits, the 62 control parameter bits are latched into a shadow register on a control pulse. The 128 mask bits are not latched.

The occurrence of a SEU in the shadow register can affect the performance of the chip. For instance, the input charge of a given polarity would not be

properly integrated and digitized if one of the polarity bits (in the preamplifier, pipeline or ADC) was upset. Unfortunately, only the shift register can be read back for verification. Since the shift register and shadow register cells share the same technology, our estimate of the SEU rate for the SVX IIe chip will be based on the measurement from the shift register cells only.

Both shift and shadow registers consist of static memory cells made of cross-coupled inverters. The regions most sensitive are the drain and source regions of the “off” NMOS and PMOS transistors, respectively (Fig. 2). The dimensions of the gate are  $l \times w = 4.8 \times 1.2$  and  $9.6 \times 1.2 \mu\text{m}^2$  for the NMOS and PMOS transistors, respectively. The combined capacitive loading determines the minimum charge required to change the state of the cell, and therefore the threshold energy  $A$ . The transistor sizes for both the shift- and shadow register cells are the same. The capacitive loading seems to be larger in the shift register cells, which would lead to a somewhat larger SEU sensitivity than for the shadow register cells. This will result in an overestimation of the SEU rate for DØ.

## 2 Cross section measurement

### 2.1 Setup

The UC Davis cyclotron generates 2 ns bunches of protons with an energy of 63.3 MeV. The bunch spacing is 44 ns. The beam profile was flat in the central core (7 cm diameter). The chips were centered well within this core. The fluence was measured with a secondary emission monitor, which was calibrated using a Faraday cup. The error on the fluence was less than 10%. This error appears as a systematic error in the cross section at each angle of incidence.

Initial runs were taken at a fluence of  $1.7 \times 10^9 \text{ cm}^{-2} \text{ s}^{-1}$ , defined with respect to an imaginary plane perpendicular to the beam. Data were taken at fluences of up to  $8 \times 10^9 \text{ cm}^{-2} \text{ s}^{-1}$ .

A 3-chip hybrid was mounted on an angular positioning device (Fig. 3). The hybrid was read out with a stand-alone version of the final data acquisition system. The shift register was read back and refreshed every five minutes. Calibration data were read out 10 times in a row after every 12 second period within the five minute interval. Data were taken in runs of 20 to 60 minutes. The integrated exposure time was about 12 hours.

The tests were performed at room temperature with no visible light sources in

the area. There was no cooling. No specific precautions were taken to shield the chips from other external influences.

## 2.2 SEU cross section

Two 3-chip hybrids were available for testing. Each hybrid was subjected to a total fluence of  $(12 \pm 1) \times 10^{13}$  protons/cm<sup>2</sup> (a total integrated dose of 16 Mrad). The hybrids were irradiated at various angles of incidence to test the angular dependence of the SEU cross section (Fig. 3). No significant dependence on the  $\phi$  angle was found. This observation justifies combining the measurements at  $\phi = 90$  and  $\phi = 0$ . The results are listed in Table 1. The cross section shows an increase with incident beam angle  $\theta$ , ranging from  $(0.4_{-0.3}^{+0.5}) \times 10^{-16}$  cm<sup>2</sup>/bit at  $\theta = 0^\circ$  (normal incidence) to  $(2.7_{-0.9}^{+1.2}) \times 10^{-16}$  cm<sup>2</sup>/bit at  $\theta = 80^\circ$ . The quoted errors are statistical only; a systematic error of 10% should be added for the calibration of the beam flux.

While the SEU rate might be expected to increase with accumulation of total integrated dose, especially as components approach failure, no increase of the cross section with time or accumulated dose was observed in this test.

No single event latchups were recorded during the test. This sets an upper limit on the SEL cross section of  $4.13 \times 10^{-15}$  cm<sup>2</sup>/chip at 95% CL.

The next generation of the SVX chip, SVX3, has been tested for SEU cross section by the CDF collaboration at the same facility [11]. The SVX3 has an analog front end, laid out using 0.8  $\mu$ m design, and a digital back end in 1.2  $\mu$ m design. The dimensions of the back end cells of the SVX3 are the same as those of the SVX IIe. The cross sections measured by CDF for the 1.2  $\mu$ m back end cells were  $(2.4_{-1.5}^{+4.2}) \times 10^{-16}$  cm<sup>2</sup>/bit and  $(6.0_{-3.8}^{+10.6}) \times 10^{-16}$  cm<sup>2</sup>/bit at 0 and 80 degrees respectively, based on a single event at each angle. These measurements are consistent with the cross sections presented in this paper. The cross sections for the smaller feature size front end cells were an order of magnitude higher, which is consistent with current models [6].

## 3 Expected SEU rates at DØ in Run 2

To predict the rate at DØ, the radiation background at DØ was estimated using GEANT 3.21 with GCALOR simulations [13–15].

The SMT consists of 6 barrels interspersed with a total of 12 disks (“F-disks”) between  $|z| = 0$  cm and  $|z| = 53$  cm. The barrels each have four layers at radii between  $r_\perp = 2.7$  and  $r_\perp = 9.4$  cm. The readout chips of the F-disks are

at a radius of  $r_{\perp} = 10$  cm. In addition, there are four disks (“H-disks”) at  $z = \pm 100$  cm and  $z = \pm 120$  cm. The readout chips for the H-disks are at a radius of  $r_{\perp} = 25$  cm (Table 2).

Since upsets in the shift registers of the chips will not affect the performance of the chip, only the 62 shadow register bits are taken into account when estimating the SEU rate.

We have used the combined cross section from the measurements at 70 and 80 degrees incident angle to estimate an upper limit on the rate. The values at 70 and 80 degrees agree well enough that their combination for this purpose is valid. The combined cross section is  $(2.6 \pm 0.7) \times 10^{-16} \text{cm}^2/\text{bit}$ . From the one-parameter Bendel fit we derive a threshold energy  $A = 36.4_{-0.6}^{+0.7}$  MeV and an asymptotic cross section  $\sigma_{\infty} = (2.9_{-0.7}^{+0.8}) \times 10^{-15} \text{cm}^2/\text{bit}$ .

At Tevatron design luminosity,  $\mathcal{L} = 2 \times 10^{32} \text{cm}^{-2}\text{s}^{-1}$ , the expected background rates for particles with  $E > 1$  MeV are given in Table 2. The error on the particle fluxes is about 20%. The charged hadron (excluding protons) and proton fluxes are roughly independent of the  $z$ -position along the beam axis. The charged hadron flux dominates the background radiation in the barrel region. From measurements of the leakage currents in the CDF Run 1 detector it was seen to decrease with increasing radius  $r_{\perp}$  as about  $r_{\perp}^{-1.7}$  [16]. The most probable energies of the background charged hadrons and protons are about 200 MeV and less than 100 MeV, respectively. To estimate the rates at  $D\bar{O}$  we have folded the cross section as given by the Bendel formula with the energy spectra for protons and charged hadrons derived from the background simulation, taking into account the factor 2 between the pion and proton cross sections [6]. The use of the high-angle cross section and the overestimation of the high-energy cross section by the one-parameter Bendel model means that our result will be a very conservative estimate.

While neutrons dominate the spectrum at large  $z$ , these neutrons mostly have energies that are too low to cause upset. The flux of neutrons with energies over the threshold energy is about two orders of magnitude lower than the flux of charged hadrons and is neglected in the estimation of the expected upset rate at  $D\bar{O}$ .

Using these numbers, the expected SEU rate for the  $D\bar{O}$  SMT is  $(2.5 \pm 0.6) \times 10^{-4} \text{s}^{-1}$ , which corresponds to between 16 and 27 upsets per full day of uninterrupted running. The rates are broken down by radial position in Table 2. The mean time between upsets is 1.1 hours. These numbers represent a very generous upper limit. This upset rate does not pose any serious problem for detector operation and data integrity. The number of chips that would be upset before a new general chip initialization takes place (a typical Tevatron store lasts less than 24 hours) represents only a small fraction of the total

number of chips. Moreover, some of the most serious symptoms of a shadow register upset, such as incorrect chip ID or ADC pedestal shifts, are constantly monitored and will lead to an immediate re-initialization of the corresponding chip.

## 4 Radiation effects

During SEU testing, the chips received doses of up to 16 Mrad<sup>1</sup>. While the download and readback functionality remained stable, the readout of the chips failed before receiving the complete dose.

The chips on the hybrid are read out in sequence: chip 0, chip 1, chip 2.

All chips showed a gradual increase in pedestal level for each channel of about 20%, starting from 43 counts on the on-board ADC to a level of 52 to 56 counts.

After sustaining doses of over 3 Mrad, the chips started to fail, the last chip in the readout chain failing first. Failure was indicated by a sharp rise in the pedestal level for each channel of more than 200% up to saturation of the ADC (Fig. 5). A few tenths of Mrads after the rise in pedestal level, first a few and then all channels of the chips read back data with a fixed value of 0.

The first chip to fail on each hybrid was chip 2, after doses of about 3.8 Mrad and 3.3 Mrad for hybrids A and B, respectively. Chips 1 and 0 on hybrid B failed after 4.3 and 4.5 Mrad, respectively. On hybrid A, chip 1 showed only a smooth pedestal increase up to a dose of about 4.2 Mrad, and neither chip 1 nor chip 0 failed completely during the entire test. Failure of one chip did not affect the other chips on the hybrid.

During calibration runs and overnight running without beam, the chips annealed to lower pedestal levels. Over the course of 5 hours running, the pedestal level on Chip 0 on the first hybrid decreased by about two counts. Chip 1 recovered from runaway pedestals up to 200 counts back to about 60 counts, still well higher than any other chip. Chip 2 was already reading back data at a fixed value of zero at this point (Fig. 6).

The expected dose rates at the DØ SMT in Run 2 are [17]:

- Layer 1 ( $r_{\perp} = 2.7cm$ ): 0.21-0.43Mrad/ $fb^{-1}$
- Layer 2 ( $r_{\perp} = 4.5cm$ ): 0.09-0.19Mrad/ $fb^{-1}$

---

<sup>1</sup> Using a conversion factor of  $7.43 \times 10^6$  protons/rad, based on the energy loss for a 63MeV proton in silicon.

- Layer 3 ( $r_{\perp} = 6.6\text{cm}$ ):  $0.05\text{-}0.09\text{Mrad}/fb^{-1}$
- Layer 4 ( $r_{\perp} = 9.4\text{cm}$ ):  $0.03\text{-}0.05\text{Mrad}/fb^{-1}$

The planned integrated luminosity for this detector is  $2\text{--}4fb^{-1}$ . The expected integrated doses are therefore well below the limit for the SVX IIe chips, even for the detector layer closest to the beam pipe.

## 5 Conclusions

The tests done at the UC Davis cyclotron show that there is no need for concern regarding the SEU sensitivity of the SVX IIe readout chips in the SMT for the first phase of DØ Run 2.

- The SEU cross section for 63 MeV protons in the SVX IIe chip increases from about  $(0.4_{-0.3}^{+0.5}) \times 10^{-16}\text{cm}^2/\text{bit}$  at normal incidence to about  $(2.7_{-0.9}^{+1.2}) \times 10^{-16}\text{cm}^2/\text{bit}$  at 80 degrees incident beam angle.
- The maximum expected upset rate for the SMT is about 21 upsets per 24 hours of uninterrupted running at design luminosity. This poses no problems for operation of the detector.
- The chips performed without problems up to integrated radiation doses of over 3 Mrad, well beyond the expected doses for this detector (maximally 1.7 Mrad).

## 6 Acknowledgments

We wish to acknowledge the contributions of R. Yarema for bringing the SEU problem to our attention and T. Zimmerman for information about the SVX IIe circuit. We thank the DØ Silicon Detector Upgrade group for providing the chips and readout system used in this test. We thank Dr. C. Castaneda and the UC Davis cyclotron staff for assistance during the run and the cyclotron management for granting development time.

## References

- [1] The DØ Collaboration. The DØ Upgrade. The detector and its physics. FERMILAB-PUB-96-357, 1996.
- [2] The DØ Collaboration. The DØ Silicon Tracker Technical Design Report. DØ internal note 2169, Fermilab, 1994.

- [3] R.J. Yarema *et al.* A Beginners Guide to the SVX II Chip. Fermilab-TM-1892, Fermilab, 1994.
- [4] Crocker Nuclear Laboratory, Davis, California USA. The proton radiation test beam at the UC Davis Crocker Nuclear Laboratory (CNL) was set up and instrumented through a joint effort of CNL and the U.S. Naval Research Laboratory.
- [5] P.E. Dodd *et al.* Impact of Technology Trends on SEU in CMOS SRAMs. *IEEE Trans. Nucl. Sci.*, 43(6):2797–2804, 1996.
- [6] M. Huhtinen and F. Faccio. Computational method to estimate single event upset rates in an accelerator environment. *Nucl. Instrum. Meth.*, A450:155–172, 2000.
- [7] W.L. Bendel and E.L. Petersen. Proton upsets in orbit. *IEEE Trans. Nucl. Sci.*, NS-30(6):4481–4485, December 1983.
- [8] Edward L. Petersen. Approaches to Proton Single-Event Rate Calculations. *IEEE Trans. Nucl. Sci.*, 43(2):496–504, 1996.
- [9] A. Akkerman, J. Barak, J. Levinson, and Y. Lifshitz. The Effect of the Angle of Incidence on Proton Induced Single Events in Devices - A Critical Assessment by Modeling. *IEEE Trans. Nucl. Sci.*, 45(3):1617–1623, 1998.
- [10] R.A. Reed, P.J. McNulty, and W.G. Abdel-Kader. Implications of Angle of Incidence in SEU Testing of Modern Circuits. *IEEE Trans. Nucl. Sci.*, 41(6):2049–2054, 1994.
- [11] G.P. Grim *et al.* Measurement of SEU cross sections in the CDF SVX3 ASIC using 63-MeV protons. *Nucl. Instrum. Meth.*, A447:160–166, 2000.
- [12] T. Zimmerman *et al.* The SVX II Readout Chip. *IEEE Trans. Nucl. Sci.*, NS-42 (4):803–807, 1995.
- [13] R. Brun and F. Carminati. GEANT Detector Description and Simulation Tool. CERN Program Library Long Writeup W5013, September 1993.
- [14] C. Zeitnitz and T.A. Gabriel. The GEANT-CALOR Interface User's Guide. URL: [http://dipmza.physik.uni-mainz.de/~zeitnitz\\_c/gcalor.html](http://dipmza.physik.uni-mainz.de/~zeitnitz_c/gcalor.html), October 1996.
- [15] E. Shabalina and V. Sirotenko. Radiation damage effects on the forward H-disks of DØ silicon tracker. DØ internal note 2800, Fermilab, 1995.
- [16] P. Azzi *et al.* Radiation Damage Experience at CDF with SVX'. *Nucl. Instrum. Meth.*, A383:155–158, 1996.
- [17] F. Lehner and S. Choi. What do we know about radiation damage in silicon detectors? DØ internal note 3803, Fermilab, 2000.

$\theta$	$\phi$	Fluence ( $\times 10^{13} \text{cm}^{-2}$ )	Upsets per $3 \times 190$ bits	$\sigma$ ( $10^{-16} \text{cm}^2/\text{bit}$ )
0	90	3.05	0	$< 1.72(95\%CL)$
180	90	4.57	1	$0.38^{+0.52}_{-0.27}$
35	90	6.20	0	$< 0.87(95\%CL)$
70	90	2.21	4	$3.17^{+1.87}_{-1.33}$
70	0	4.88	6	$2.16^{+1.00}_{-0.76}$
80	0	3.90	6	$2.66^{+1.24}_{-0.94}$
0 + 180	90	7.62	1	$0.24^{+0.33}_{-0.17}$
70 0 + 90		7.09	10	$2.47^{+0.87}_{-0.70}$

Table 1

Number of SEU occurrences and measured cross section as a function of the incident beam angle.

	$r_{\perp}(cm)$	$ z (cm)$	# SVX IIe chips	flux ( $cm^{-2}s^{-1}$ )	expected SEU rate ( $s^{-1} \times 10^{-4}$ )
Layer 1	2.7	0 - 38	360	$3 \times 10^4$ p; $1 \times 10^6$ $h^{\pm}$	0.85
Layer 2	4.5	0 - 38	648	$1 \times 10^4$ p; $3 \times 10^5$ $h^{\pm}$	0.46
Layer 3	6.6	0 - 38	720	$5 \times 10^3$ p; $2 \times 10^5$ $h^{\pm}$	0.34
Layer 4	9.4	0 - 38	1296	$1 \times 10^3$ p; $1 \times 10^5$ $h^{\pm}$	0.30
F-disks	10	0 - 53	2016	$1 \times 10^3$ p; $1 \times 10^5$ $h^{\pm}$	0.47
H-disks	25	100, 120	1152	$3 \times 10^3$ p; $1 \times 10^4$ $h^{\pm}$	0.03
TOTAL			6192		$2.5 \pm 0.6$

Table 2

Expected particle fluxes and SEU rates in  $D\bar{O}$  at  $\mathcal{L} = 2 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$ . The charged hadron flux does not include protons, which have to be added separately. The estimated error on the particle fluxes is about 20%.

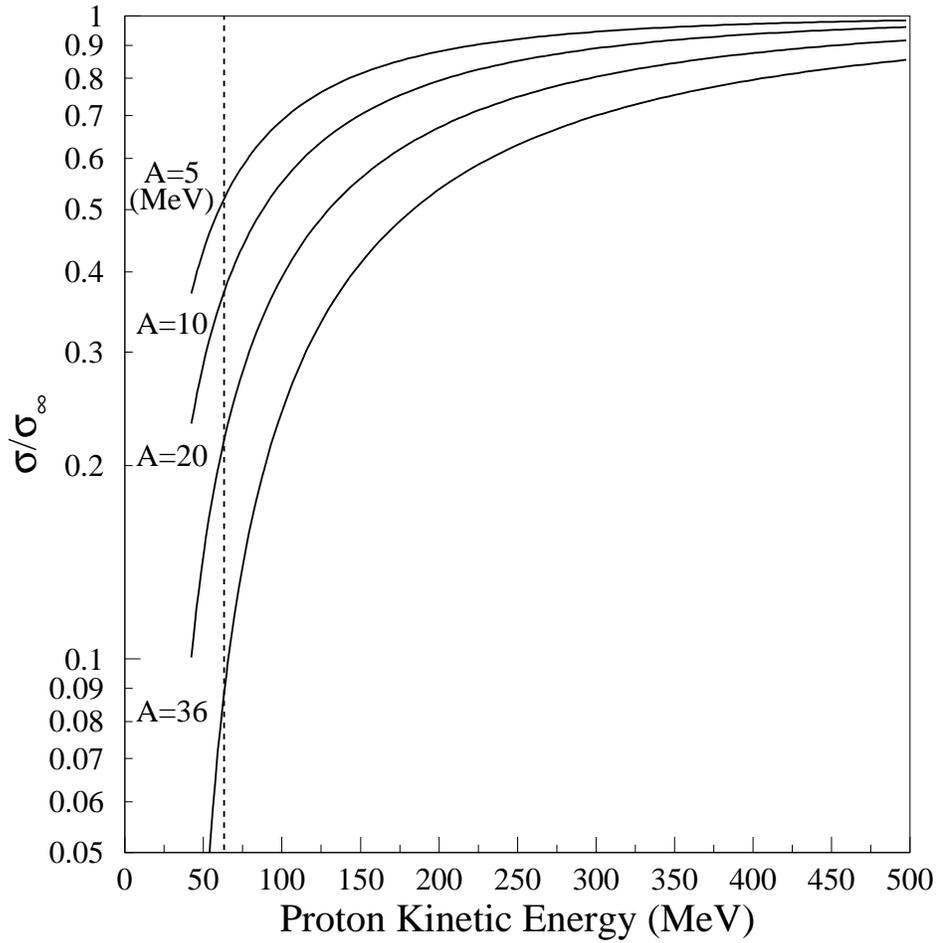


Fig. 1. Normalized Bendel curves for four values of the threshold energy  $A$ . The dashed line indicates a proton energy of 63 MeV. For large threshold energies the asymptotic cross section can be significantly higher than that at 63 MeV.

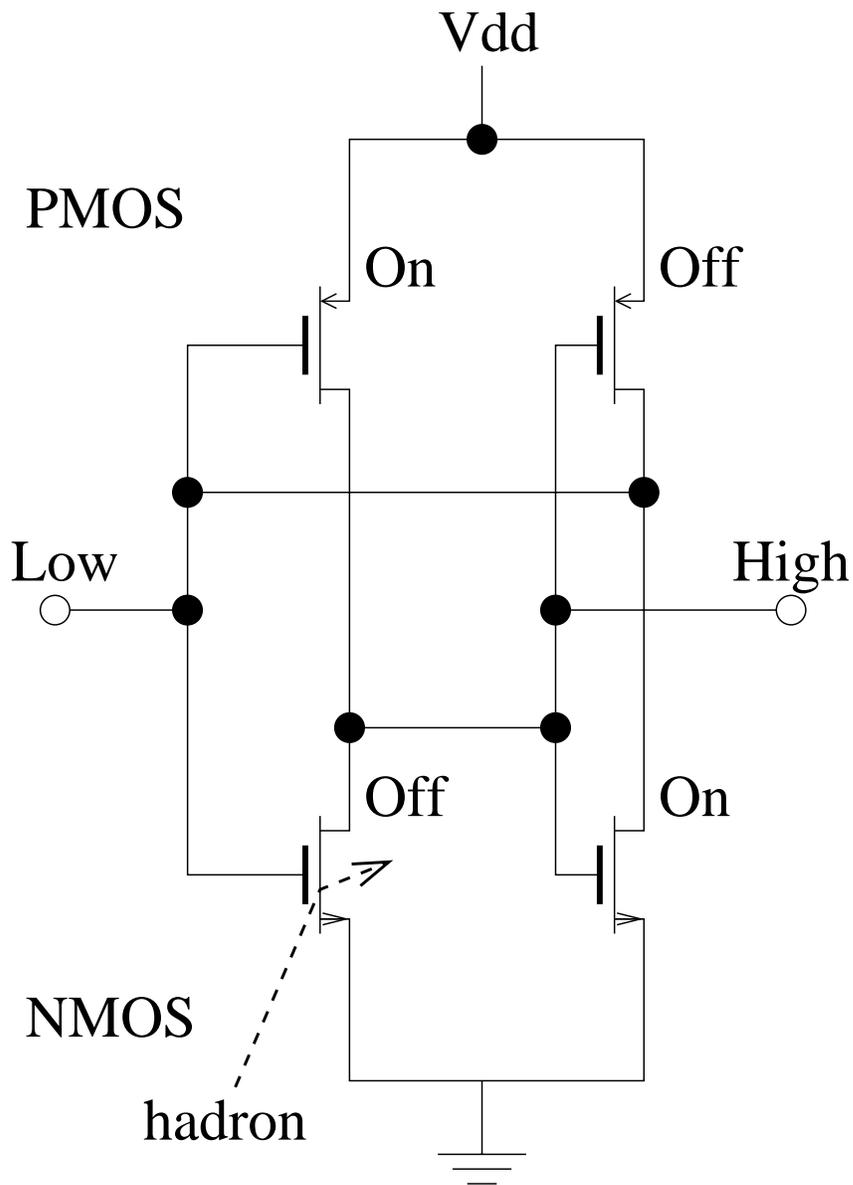


Fig. 2. Simplified schematic of the SVX IIe CMOS memory cells showing a hadron interacting near the "off" NMOS transistor.

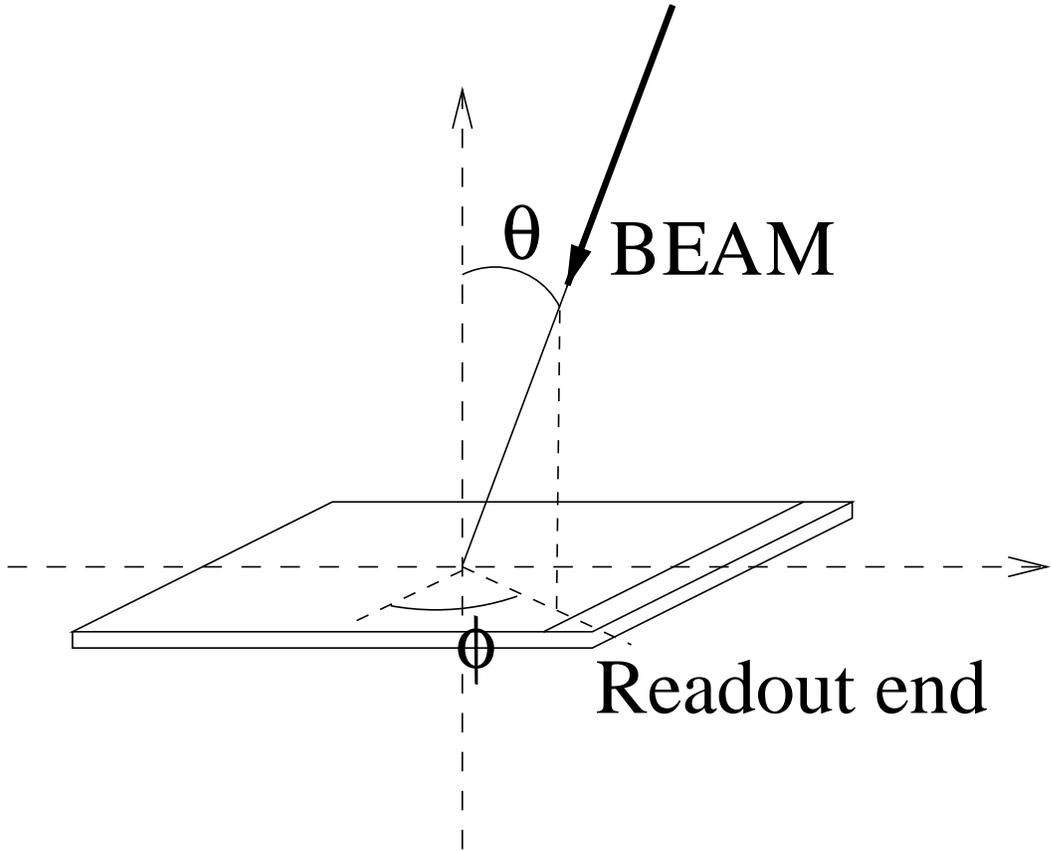


Fig. 3. Test setup showing the beam angle of incidence with respect to the SVX IIe chip.

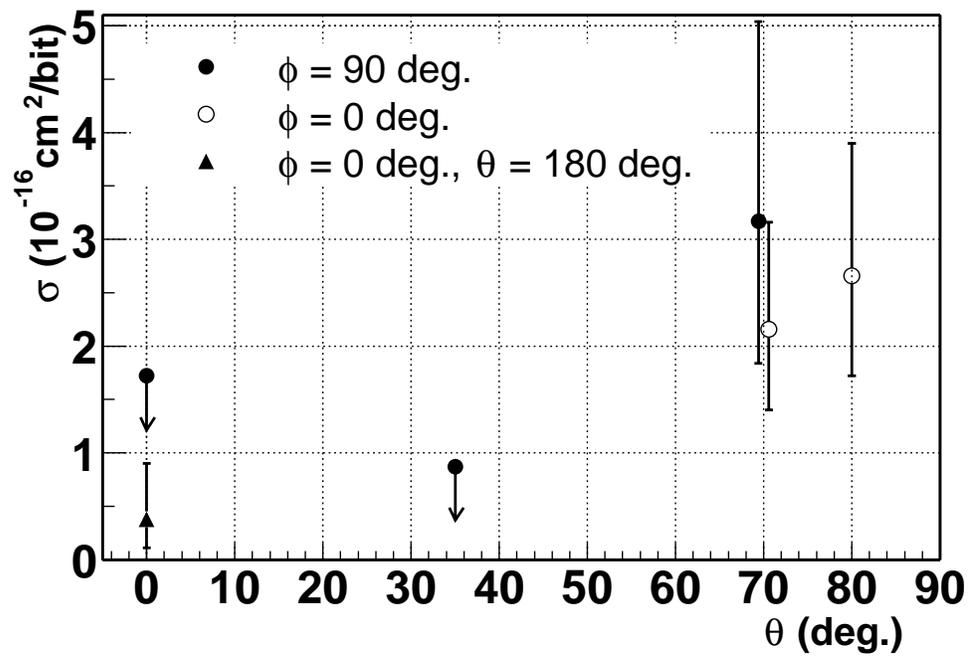


Fig. 4. Measured SEU cross section as a function of incident beam angle.

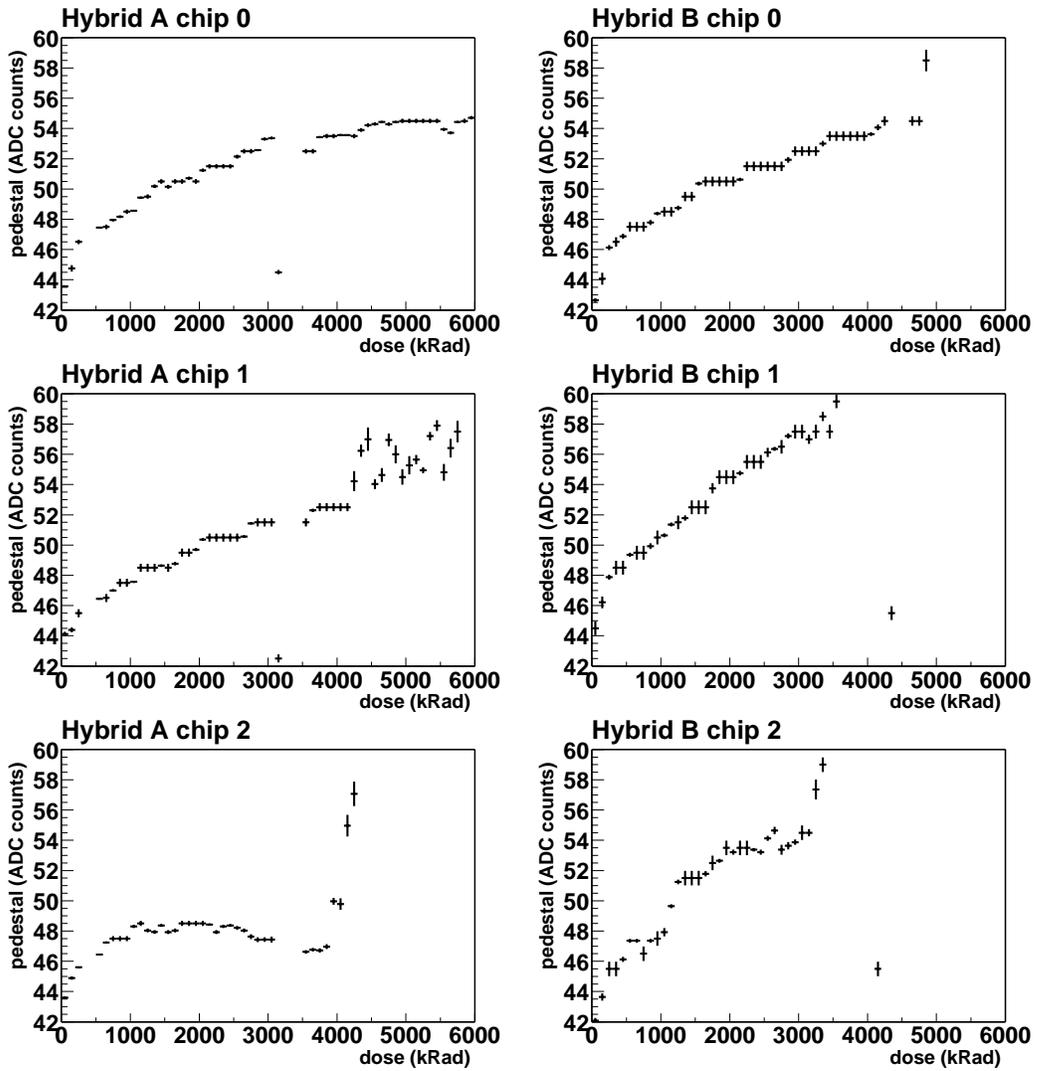


Fig. 5. Average pedestal per chip variation versus integrated dose.

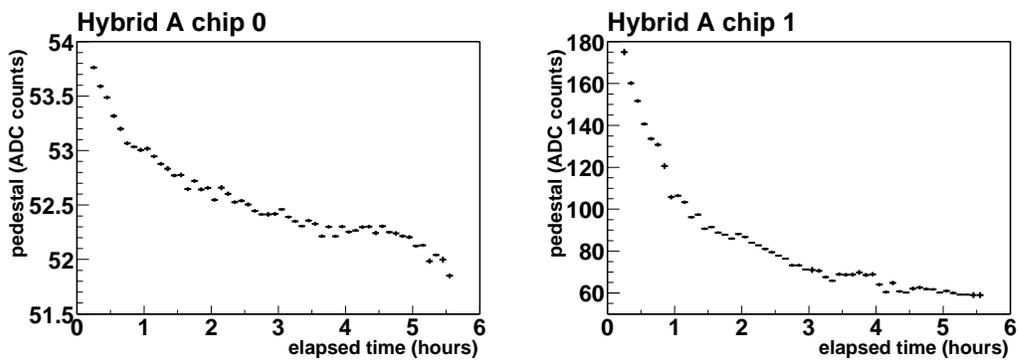


Fig. 6. Observed annealing in average chip pedestal for chips 0 and 1 on hybrid A, after 16 Mrad exposure.