



## Development of a High Density Pixel Multichip Module at Fermilab

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### Abstract

At Fermilab, both pixel detector multichip module and sensor hybridization are being developed for the BTeV experiment. The BTeV pixel detector is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating the two together. This method offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor material. This paper presents strategies to handle the required data rate and performance results of the first prototype and detector hybridization.

### Introduction

At Fermilab, the BTeV experiment has been approved for the C-Zero interaction region of the Tevatron [1]. The tracker detector for this experiment will be a pixel detector composed of 62 pixel planes of approximately 100x100 mm<sup>2</sup> each, assembled in 31 stations. The planes are located perpendicular to the colliding beam with pixels as close as 6 mm to the beam. Each plane is formed by an arrangement of multichip modules with three different lengths: 100 mm, 60 mm and 48 mm. The modules are formed by up to 9 pixel readout chips bump bonded to a single sensor. The modules on opposite faces of the same pixel station are assembled perpendicularly in relation to each other (see Figure 1).

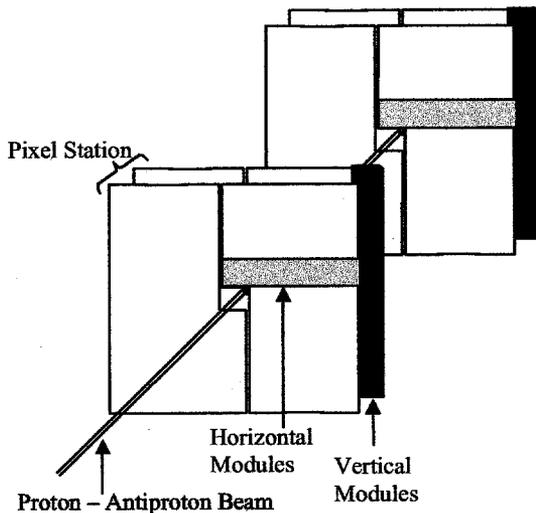


Figure 1 – Pixel Station

The pixel detector will be employed for on-line track finding for the lowest level trigger system and, therefore, the pixel readout chips will have to read out all detected hits. This requirement imposes a severe constraint on the design of the readout chip, the hybridized module, and the data transmission to the data acquisition system.

The multichip modules must conform to special requirements dictated by BTeV [1]: the pixel detector will be inside a strong magnetic field (1.6 Tesla in the central field), the flex circuit and the adhesives cannot be ferromagnetic, the pixel detector will also be placed inside a high vacuum environment, so the multichip module components cannot outgas, the radiation rates (around 3 Mrad per year) and temperature (-5° C) also impose severe constraints to the pixel multichip module packaging design.

### Pixel Module Readout

The pixel module readout must allow the pixel detector to be used in the lowest level experiment trigger. Our present assumptions are based on simulations that describe the data pattern inside the pixel detector [3]. The parameters used for the simulations are: luminosity of 2x10<sup>32</sup> cm<sup>-2</sup>s<sup>-1</sup> (corresponds to an average of 2 interactions per bunch crossing), pixel size of 400x50 μm<sup>2</sup>, threshold of 2000 e<sup>-</sup> and a magnetic field of 1.6 Tesla.

Figure 2 shows a sketch of the 40 chips that may compose a pixel half plane. The beam passes on the place represented by the black dot. These numbers assume specific data format and chip size. The rows in Figure 2 represent pixel multichip modules. For this discussion the modules are numbered from 1 to 5 from top to bottom. The chips are labeled from a to i from left to right. Module 4 is the busiest pixel module. The chip e in module 4 and chip d in module 5 are the busiest chips.

	a	b	c	d	e	f	g	h	i
Module 1 →	11	13	17	17	20	18	16	13	8
Module 2 →	11	18	26	31	39	33	25	18	12
Module 3 →	16	20	37	61	76	59	39	26	18
Module 4 →	17	35	63	141	234	130	65	36	16
Module 5 →	23	35	74	234					

• ← Beam

Figure 2 – Average Bit Data Rate, in Mbit/s

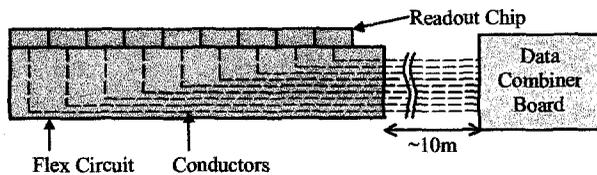
Table 1 presents the required bandwidth per module. From this table we see that each half pixel plane requires a bandwidth of approximately 1.8 Gbit/s.

	<i>Req. Bandwidth</i>
<i>Module 1</i>	133
<i>Module 2</i>	213
<i>Module 3</i>	352
<i>Module 4</i>	737
<i>Module 5</i>	366
<i>Total</i>	<i>1801</i>

**Table 1 – Half Plane Required Bandwidth, in Mbit/s**

**Proposed Readout Architecture**

The system design is evolving and it is not finalized yet. The present proposed scheme is the following. The pixel multichip modules connect to a Data Combiner board. The Data Combiner board merges the data from the pixel modules mounted in a half plane and sends the data for the trigger system. The readout chips in the pixel module use Low Voltage Differential Signal (LVDS) point-to-point connections to transmit the data to the Data Combiner board. Figure 3 shows a sketch of the proposed readout. For another proposal see [3].



**Figure 3 – Pixel Module Point-to-Point Connection**

The number of differential wires required to read out the pixel module is associated with the readout clock frequency. All chips in a module are connected to the same readout clock.

Table 2 shows the number of differential wires required to read out all chips of the busiest module (number 4) for four different clock frequencies. The output of the chips is configurable to different numbers of differential pairs to accommodate different data rate requirements.

		<i>Clock Frequency in MHz</i>			
		<i>53</i>	<i>106</i>	<i>159</i>	<i>212</i>
<i>Readout chip in module 4</i>	<i>a</i>	4	2	2	2
	<i>b</i>	6	4	2	2
	<i>c</i>	10	6	4	4
	<i>d</i>	22	12	8	6
	<i>e</i>	36	18	12	10
	<i>f</i>	20	10	8	6
	<i>g</i>	10	6	4	4
	<i>h</i>	6	4	2	2
	<i>i</i>	3	2	2	2
	<i>Total</i>	<i>117</i>	<i>64</i>	<i>44</i>	<i>38</i>

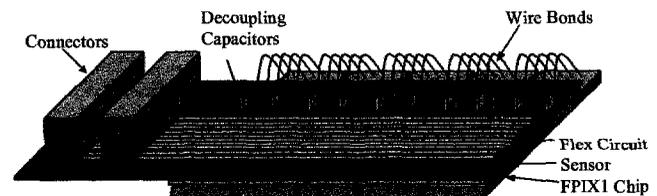
**Table 2 – Number of Conductors in the Flex Circuit**

Table 2 shows that increasing the clock frequency above 159 MHz will not significantly reduce the number of

conductors in the flex circuit. This is because a chip requires at least one differential pair of wires to transmit its data, even if the bandwidth of this path is not fully utilized. This estimate uses a safety margin of 4 times more bandwidth (relative to Table 1) to account for simulation uncertainties. In addition to the readout conductors, several control and clock signals are distributed to the chips in the module. The total number of wires requires a high density flex circuit with traces and spaces as small as 75 μm to fit in the small area available.

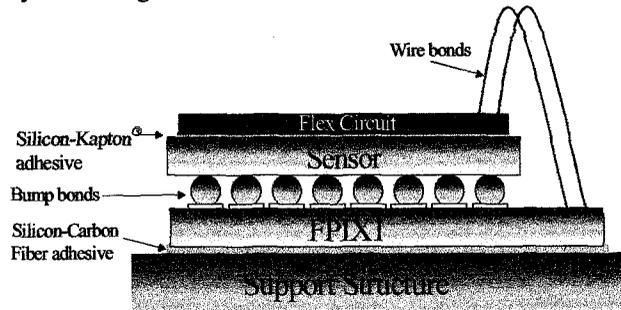
**Multichip Module Prototype Packaging**

This section describes the development of the pixel multichip module prototype packaging (as sketched in Figure 4). This design uses the FPIX1 version of the Fermilab Pixel readout chip [2].



**Figure 4 – Sketch of the Pixel Multichip Module**

The pixel multichip module packaging is composed of three layers, as depicted in Figure 5. The pixel readout chips form the bottom layer. The back of the chips is in thermal contact with the station supporting structure, while the other side is flip-chip bump bonded to the silicon pixel sensor. The clock, control, and power pad interfaces of FPIX1 extend beyond the edge of the sensor.



**Figure 5 – Sketch of the Pixel Multichip Module “Stack”**

The Kapton® interconnect circuitry (flex circuit) is placed on the top of this assembly and the FPIX1 pad interface is wire-bonded to the circuit. The circuit then extends to one end of the module where low profile connectors interface the module to the data acquisition system. The large number of signals in this design imposes space constraints and requires aggressive design rules, such as 25 μm trace width, trace-to-trace clearance of 25 μm, and 5 μm trace thickness.

This packaging requires a flex circuit with four layers of copper traces (as sketched in Figure 6). The data, control and clock signals use the two top layers, power uses the third layer and ground and sensor high voltage bias use the bottom layer. The flex circuit has two power traces, one analog and one

digital. These traces are wide enough to guarantee that the voltage drop from chip to chip is within the FPIX1  $\pm 5\%$  tolerance. The decoupling capacitors in the flex circuit are placed as close as possible to the pixel chips. The trace lengths and vias that connect the capacitors to the chips are minimized as much as possible to reduce the interconnection inductance.

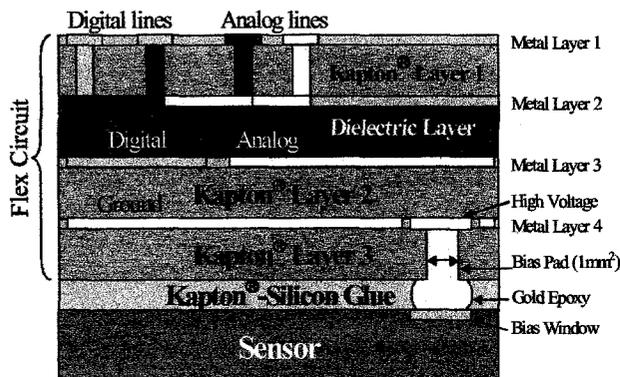


Figure 6 – Sketch of Flex Circuit Cross Section

To minimize coupling between digital and analog elements, signals are grouped together into two different sets. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

#### High Voltage Bias

The pixel sensor is biased with up to 1000 VDC through the flex circuit. The coupling between the digital traces and the bias trace has to be minimized to improve the sensor noise performance. To achieve this, the high voltage trace runs in the fourth metal layer (ground plane, see Figure 6) and below the analog power supply trace. The high voltage electrically connects to the sensor bias window through gold epoxy. A window in the fourth metal plane guarantees no arcing between the high voltage via and the ground plane. A Kapton® layer in the bottom of the flex circuit isolates the ground in the fourth metal layer of the flex circuit from the high voltage of the pixel sensor.

#### First Prototype Pixel Module

Figure 7 shows a picture of the first prototype of the pixel module. It is composed of a pixel sensor bump-bonded to five FPIX1 readout chips and a four layer high density flex circuit [3].

In this prototype the flex interconnect is located on the side of the readout chips instead of on the top of the sensor (as in the baseline design). The pixel sensor used is oversized; it can be bump-bonded to a total of 16 readout chips.

This pixel module has been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end of the readout chip with a pulse generator and reading out the hit data through a logic state analyzer. Data of just four readout chips is available because one of the chips failed. The results for one specific threshold are summarized in Table 3.

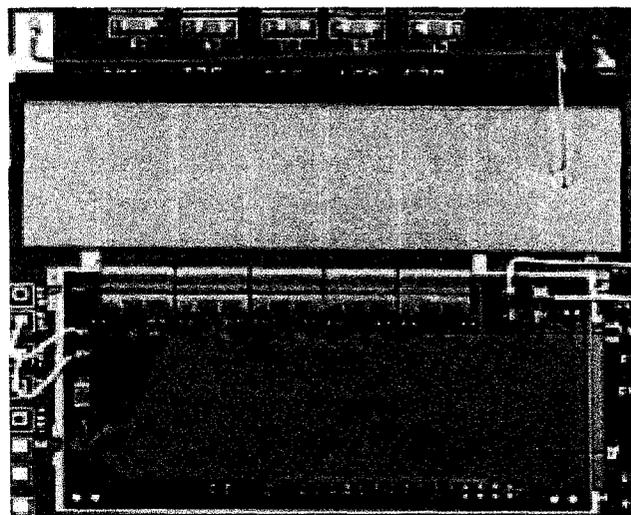


Figure 7 – Prototype Pixel Module

Chip	1	2	3	4
Threshold Mean	1649	1406	1589	2865
Threshold Sigma	254	307	222	250
Noise Mean	62	53	49	62
Noise Sigma	16	13	11	11

Table 3 – Performance of the Five Chip Module (in  $e^-$ )

The comparison of these results with the results of a single FPIX1 chip shows no noticeable degradation in performance [4]. Figure 8 shows the hit map of a pixel chip in the 5-chip pixel module using a radioactive source (Sr 90). Furthermore, tests with a deadtimeless mode, where the charge injected into the front end is time-swept in relation to the readout clock also does not reveal any degradation in performance, indicating no crosstalk problems between the digital and analog sections of the FPIX1 and flex circuit.

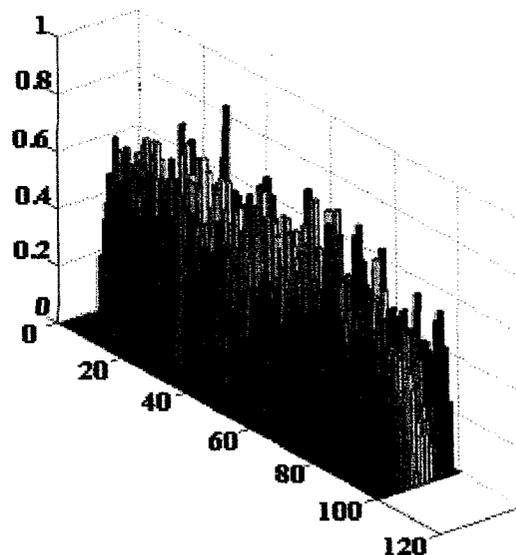


Figure 8 – Pixel Chip Hit Map

### Results of the Hybridization to Pixel Sensors

The hybridization approach pursued offers maximum flexibility. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip mating technology. We have tested three bump bonding technologies: indium, fluxed solder, and fluxless solder. Real sensors and readout chips were indium bumped at both the single chip or wafer level by BOEING, NA. Inc (Anaheim, CA) and Advance Interconnect Technology Ltd. (Hong Kong) with satisfactory yield and performance.

We have recently received a new batch of single chip detectors and modules bumped bonded at AIT. Figure 9 is a Scanning Electron Micrograph (SEM) showing the indium bumps deposited on the readout chip. The bumps are about 10  $\mu\text{m}$  high and 12  $\mu\text{m}$  wide at the base. Figure 10 is a picture of our new 5-chip module.

We have also conducted tests on dummy detectors to evaluate eutectic Pb/Sn solder. The vendor, MCNC (Research Triangle Park, NC), together with UNITIVE Electronics (Research Triangle Park, NC), produced the dummy parts, and then carried on with the bumping process. The detectors are composed of channels that are a number of daisy-chained bumps at 50  $\mu\text{m}$  pitch connected to probe pads at an edge of the dummy detector. We characterized the bump yield by measuring the resistance of each channel, and (to check for shorts) the resistance between neighboring channels.

Both fluxed and fluxless solder bumps have been studied. We found much better results using the fluxless process. The yield from the fluxed process is poor. For the fluxless assemblies, a process called Plasma Assisted Dry Soldering (PADS) [5] is used. The bumped chip wafer (top plates of the dummies) and un-bumped substrate wafer (bottom plates of the dummies with only under-bump metallization put on) were diced and tacked together (flip-chip assembly) before being treated in the PADS process. The solder was then reflowed at 250°C. After being reflowed, the detectors were rinsed with methanol and dried in air. The diameter of the bumps is approximately 40  $\mu\text{m}$ , and the height is approximately 15  $\mu\text{m}$  after mating. We estimate that the single solder bump resistance is less than 1  $\Omega$ .

We have previously reported [3] a bump yield of 99.95% or  $4.5 \times 10^{-4}$  failure/bump. The causes of the failures have been identified and solutions have been adopted to overcome these problems. This has led to changes in the bumping process.

One of the main problems identified was the oxidization of the Under Bump Metallization (UBM) before the solder bumps were put on the part [6]. This thin oxide layer prevents the formation of a good joint until it is "broken" through by the application of an electrical voltage. To overcome this, the vendor has developed a process of gold plating the UBM which prevents the oxidization. Figure 11 shows an example of the gold plating process.



Figure 9 – Indium Bumps on the Readout Chip.

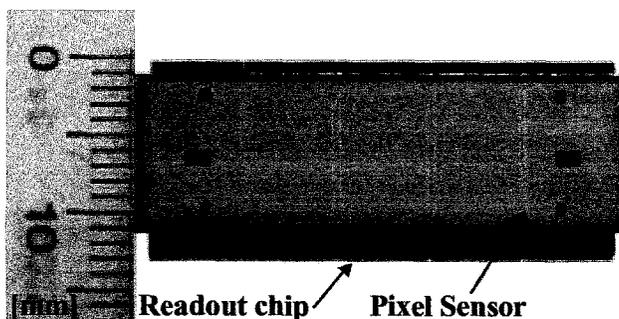


Figure 10 – 5-chip Pixel Module with Indium Bumps

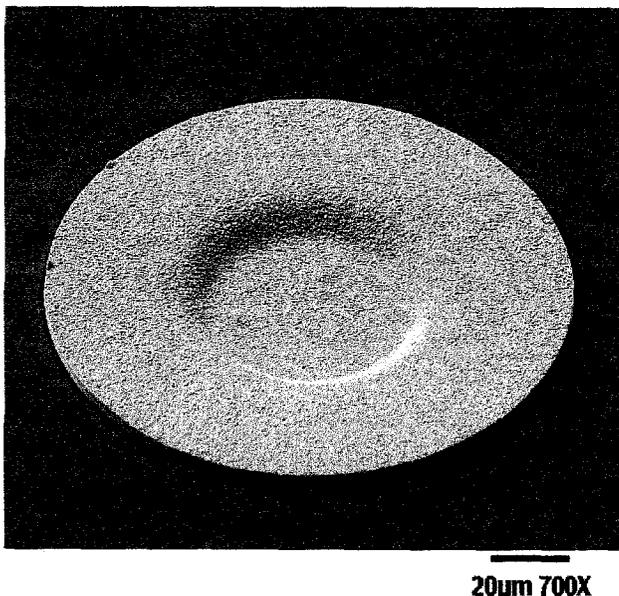
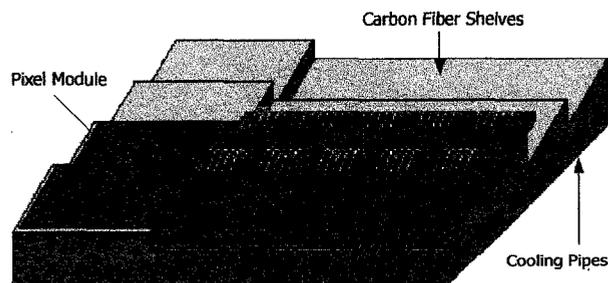


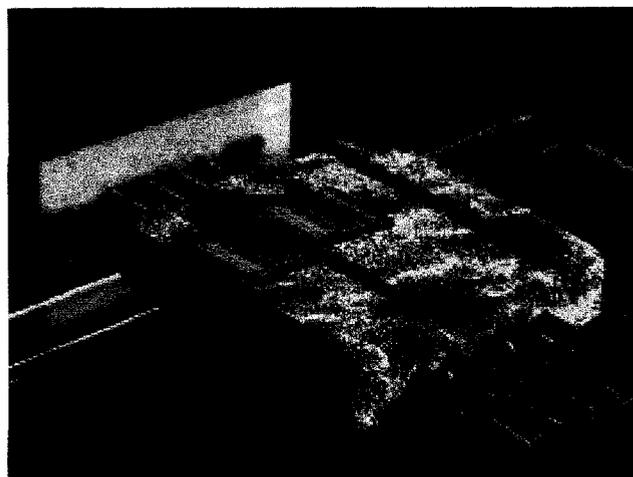
Figure 11 – Gold Plated Pad

## Future Plans

A set of stack pixel modules will be mounted to form a pixel plane (see Figure 12). The support structure is a fuzzy carbon with cooling pipes made out of embedded carbon tubes. The upper surface is then milled with shingle ramps. Figure 13 shows a cooled carbon substrate prototype provided by Energy Science Laboratories Inc. (San Diego, CA) with two chips pasted on the structure. The modules are shingled so that there is no portion of the plane that is not instrumented by pixel sensors when looking perpendicularly to the plane.



**Figure 12 – Sketch of the Pixel Module “Shingled” Support Structure**



**Figure 13 – Carbon Fiber Supporting Structure Prototype**

## Conclusions

We have described the baseline design pixel multichip module designed to handle the data rate required for the BTeV experiment at Fermilab. The present prototype has shown good electrical performance characteristics.

Indium bump bonding is proven to be capable of successful fabrication at 50  $\mu\text{m}$  pitch on real detectors. For solder bumps at 50  $\mu\text{m}$  pitch, good results have been obtained with the fluxless PADS processed detectors. The results are adequate for our needs and our tests have validated them as a viable technology.

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Kapton<sup>®</sup> is a registered trademark of DuPont Company.

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